FLUKE®

Instruction Manual

Model

4265A

Binary Programmable Power Source

P/N 310831

REV. 1 2/75

JANUARY 1973

LIMITED WARRANTY

The JOHN FLUKE MFG. CO., INC., warrants each instrument it manufactures to be free from defects in material and workmanship under normal use and service for the period of one year from date of purchase. This warranty extends only to the original purchaser. This warranty shall not apply to fuses, disposable batteries (rechargeable type batteries are warranted for 90 days), or any product or parts which have been subject to misuse, neglect, accident or abnormal conditions of operations.

In the event of failure of a product covered by this warranty, John Fluke Mfg. Co., Inc., will repair and calibrate an instrument returned to an authorized Service Facility within one year of the original purchase; provided the warrantor's examination discloses to its satisfaction that the product was defective. The warrantor may, at its option, replace the product in lieu of repair. With regard to any instrument returned within one year of the original purchase, said repairs or replacement will be made without charge. If the fault has been caused by misuse, neglect, accident or abnormal conditions of operations, repairs will be billed at a nominal cost. In such case, an estimate will be submitted before work is started, if requested.

ANY IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS SHALL BE LIMITED TO A PERIOD OF TWELVE MONTHS FROM THE DATE OF PURCHASE. THE FOREGOING WARRANTY IS IN LIEU OF ALL OTHER WARRANTIES, EXPRESS OR IMPLIED, INCLUDING BUT NOT LIMITED TO ANY IMPLIED WARRANTY OF MERCHANTABILITY, FITNESS OR ADEQUACY FOR ANY PARTICULAR PURPOSE OR USE. JOHN FLUKE MFG. CO., INC. SHALL NOT BE LIABLE FOR ANY SPECIAL, INCIDENTAL OR CONSEQUENTIAL DAMAGES, WHETHER IN CONTRACT, TORT OR OTHERWISE.

NOTE: Some states do not allow limitations on how long an implied warranty lasts, or the exclusion or limitation of incidental or consequential damages, so the above limitations or exclusion may not apply to you. This warranty gives you specific legal rights, and you may also have other rights which vary from state to state.

If any fault develops, the following steps should be taken:

1. Notify the John Fluke Mfg. Co., Inc. or nearest Service facility, giving full details of the difficulty, and include the Model number, type number, and serial number. On receipt of this information, service data or shipping instructions will be forwarded to you.

2. On receipt of the shipping instructions, forward the instrument, transportation prepaid. Repairs will be made at the Service Facility and the instrument returned, transportation prepaid.

SHIPPING TO MANUFACTURER FOR REPAIR OR ADJUSTMENT

All shipments of John Fluke Mfg. Co., Inc., instruments should be made via United Parcel Service or "Best Way"* prepaid. The instrument should be shipped in the original packing carton; or if it is not available, use any suitable container that is rigid and of adequate size. If a substitute container is used, the instrument should be wrapped in paper and surrounded with at least four inches of excelsior or similar shock-absorbing material.

CLAIM FOR DAMAGE IN SHIPMENT TO ORIGINAL PURCHASER

The instrument should be thoroughly inspected immediately upon original delivery to purchaser. All material in the container should be checked against the enclosed packing list. The manufacturer will not be responsible for shortages against the packing sheet unless notified immediately. If the instrument is damaged in any way, a claim should be filed with the carrier immediately. (To obtain a quotation to repair shipment damage, contact the nearest Fluke Technical Center.) Final claim and negotiations with the carrier must be completed by the customer.

The John Fluke Mfg. Co., Inc. will be happy to answer all application or use questions, which will enhance your use of this instrument. Please address your requests or correspondence to: JOHN FLUKE MFG. CO., INC., P.O. Box 43210, MOUNTLAKE TERRACE, WASHINGTON 98043, Atten: Sales Dept. For European Customers: FLUKE (Nederland) B.V., Zevenheuvelenweg 53, Tilburg, The Netherlands.

* For European customers, Air Freight prepaid.

John Fluke Mfg. Co., Inc. • P.O. Box 43210 • Mountlake Terrace, Washington 98043

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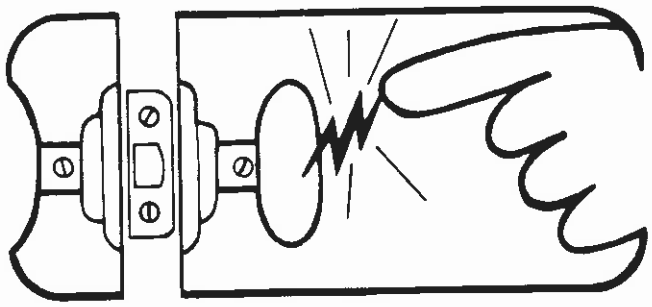
static awareness

A Message From

John Fluke Mfg. Co., Inc.

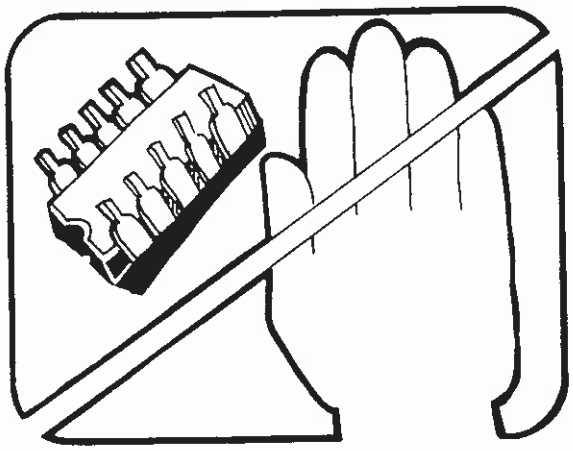


Some semiconductors and custom IC's can be damaged by electrostatic discharge during handling. This notice explains how you can minimize the chances of destroying such devices by:

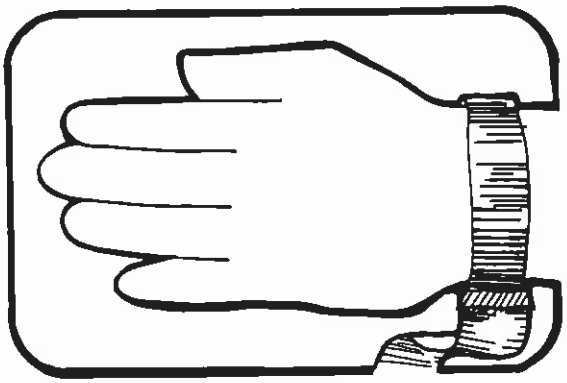
1. Knowing that there is a problem.
2. Learning the guidelines for handling them.
3. Using the procedures, and packaging and bench techniques that are recommended.

The Static Sensitive (S.S.) devices are identified in the Fluke technical manual parts list with the symbol "⊗".

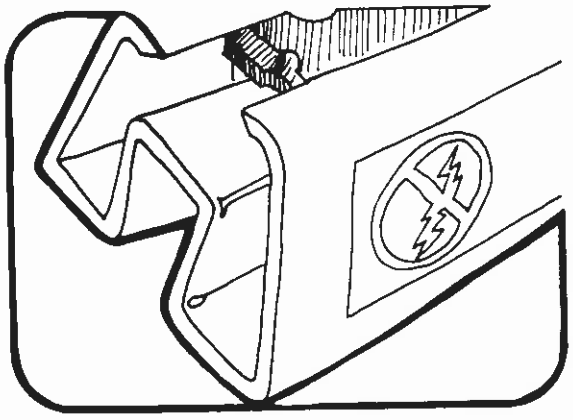
The following practices should be followed to minimize damage to S.S. devices.



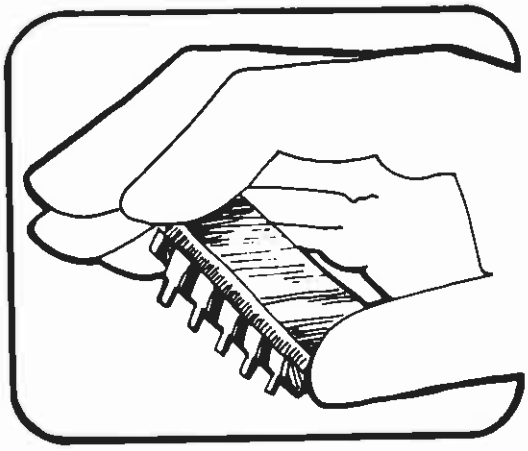
1. MINIMIZE HANDLING



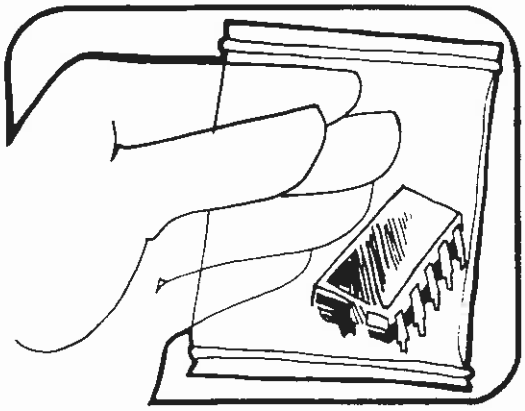
3. DISCHARGE PERSONAL STATIC BEFORE HANDLING DEVICES



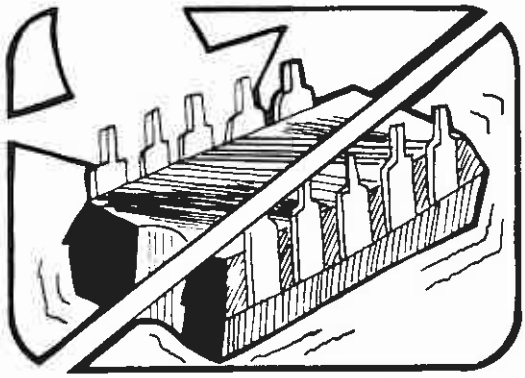
2. KEEP PARTS IN ORIGINAL CONTAINERS UNTIL READY FOR USE.



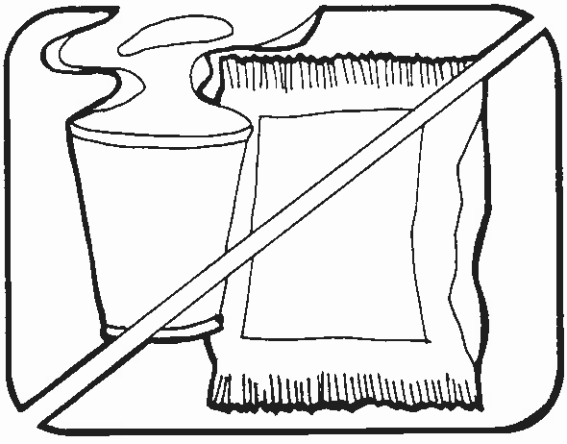
4. HANDLE S.S. DEVICES BY THE BODY



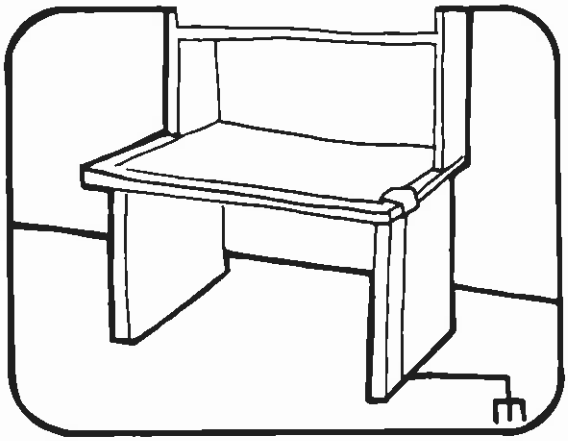
5. USE ANTI-STATIC CONTAINERS FOR HANDLING AND TRANSPORT



6. DO NOT SLIDE S.S. DEVICES OVER ANY SURFACE



7. AVOID PLASTIC, VINYL AND STYRAFOAM IN WORK AREA



8. HANDLE S.S. DEVICES ONLY AT A STATIC-FREE WORK STATION

9. ONLY ANTI-STATIC TYPE SOLDER-SUCKERS SHOULD BE USED.

10. ONLY GROUNDED TIP SOLDERING IRONS SHOULD BE USED.

Anti-static bags, for storing S.S. devices or pcbs with these devices on them, can be ordered from the John Fluke Mfg. Co., Inc.. See section 5 in any Fluke technical manual for ordering instructions. Use the following part numbers when ordering these special bags.

John Fluke Part No.	Bag Size
453522	6" x 8"
453530	8" x 12"
453548	16" x 24"
454025	12" x 15"

Section 1

Introduction & Specifications

1-1. INTRODUCTION

1-2. The Model 4265A is a programmable, bipolar dc voltage source. Output voltage is from 0 to 65.532 vdc in two ranges; 16 and 65 vdc. Programming resolution using the internal reference voltage is 1 mv on the 16 volt range and 4 mv on the 65 volt range. Output accuracy is ±.01% of the programmed level on both voltage ranges. After a 100 μsec settling time, a READY/NOT READY FLAG indicates that the output has settled to ±.01% of the programmed increment for a resistive load. The output current is rated at ±1 ampere maximum and is limited to approximately ±1.1 ampere in the event of an overload or short circuit. The sink current (milliamps) is rated at 1000-10 E_{OUT} maximum. A Programmable Current Limiter (Option −06) is available to allow programming the maximum output current to a lower level. A current limit flag indicates when a sink or source current overload exists with or without the −06 Option.

1-3. Programming requirements are compatible with DTL or TTL logic levels. Contact or relay closures can also be used. The voltage source is programmed on the low range using straight binary coding. The high range is also programmed in the same manner, but the actual output is four times the programmed level. Two's complement coding is required for negative outputs when the Isolated Control Logic (−01 Option) is installed. All programming inputs and flag outputs are available through a 50 pin Amphenol, Blue Ribbon connector located on the rear panel. A +5 vdc output is also available at this connector and is used to provide power for external programming circuitry. Negative logic is employed for programming. The logic levels are as follows:

Logic "0" = +2.0 vdc to +5.0 vdc or open circuit
Logic "1" = 0 to +0.4 vdc or short circuit to LOGIC GRD.

1-4. Three options are available to provide tailoring of the power supply to fit application requirements. These options are identified by numeric designations −03, −06, and −09. A description of each option is provided in Table 1-1. These options may be installed at the factory when the instrument is ordered or in the field at a later time.

1-5. Physically, the power source is completely solid state. Plug in printed circuit boards, with easy to reach test points and adjustments, are used for ease in servicing. The unit is forced air cooled. This results in lower component temperatures and thus higher reliability than would normally be obtained in a source of this power capability. The chassis is designed for bench top use, or it can be installed in a standard equipment rack by using the Accessory Rack Mounting Fixtures.

Table 1-1. OPTIONS

OP-TIONS	TITLE	DESCRIPTION
–01	ISOLATED CONTROL LOGIC (Now Standard)	Separates the external digital interface logic and attendant noise from the Model 4265A analog circuitry. Impedance between the interface logic and the analog circuitry is greater than 10^9 ohms, in parallel with 3 pf. It also provides a data storage that allows multiplexing of several voltage sources from one system interface register or data bus. Two's complement binary coding is required for negative outputs.
–02	FRONT PANEL DISPLAY (Now Standard)	Lamps (light emitting diodes) installed on the front panel which indicates the programmed VOLTAGE LEVEL, SIGN, CURRENT LIMIT, EXT REF, POWER ON, and STDBY conditions.
–03	EXTERNAL REFERENCE (Field Installable)	Allows the use of an external signal source in place of the internal reference voltage. Any dc or ac signal can be used that has an amplitude from 0 to ±14.5 volts and a frequency from dc to 30 kHz. Input impedance is 100K, in parallel with 70 pf.
–04	DIRECT COUPLED CONTROL LOGIC (No Longer Available)	The Direct Coupled Control Logic is no longer offered as an option to the 4200 series instruments. The Isolated Control Logic (see description above) is now standard equipment on all instruments.
–05	BLANK FRONT PANEL (No Longer Available)	The Blank Front Panel is no longer offered as an option to the 4200 series instruments. The Front Panel Display (see description above) is now standard equipment on all instruments.
–06	PROGRAMMABLE CURRENT LIMITING (Field Installable)	Programmable current limit is provided in two ranges, 100 ma and 1 ampere. Each range may be programmed in 10% increments from 10% to 110% of range.
–09	MULTI-STROBE ISOLATED LOGIC (Field Installable)	Permits any of the Fluke 4200 series Programmable Voltage Sources to be remotely controlled by a large variety of program sources such as a computer, a system coupler, as well as a Fluke Automatic Test Equipmetn System. Refer to Section 6 for details.

1-6. SPECIFICATIONS

OUTPUT VOLTAGE . . . . . 0 to ±16.383 vdc
0 to ±65.532 vdc
(Maximum output terminal voltage = ±66v minimum)

OUTPUT VOLTAGE RESOLUTION . .
16v Range . . . . . 1.0 mv
65v Range . . . . . 4 mv
(Provisions have been made to allow changing of the MSB weight to 8000 and 32000 mv by installation of a jumper in the Preamplifier.)

OUTPUT CURRENT	0 to ±1 ampere (Short circuit protected at 1.1 ampere)
CURRENT SINK CAPABILITY	I_{SINK} (ma) = 1000 – 10 E OUT (Overload protected) The Current Limit Flag is energized when a current sink overload condition occurs.
ACCURACY (15°C to 35°C, 90 days)	
16v Range	±(0.01% of program +100 uV)
65v Range	±(0.01% of program +300 uV)
STEADY STATE RIPPLE AND NOISE (10 Hz to 10 MHz bandwidth) 16v Range	500 uV rms 7mV p-p
65v Range	1 mV rms 7mV p-p
OUTPUT IMPEDANCE	0.02 milliohms @ dc; 1 ohm @ 30 kHz
EXTERNAL REFERENCE (Option –03)	
Voltage Range	0 to ±14.5 VDC or peak ac
Input Impedance	100k ohms in parallel with 70 pf
Output Voltage	
16v Range	0 to 12v rms, 17V peak
65v Range	0 to 46v rms, 66V peak
Output Current	707 ma rms, 1.0 amp peak
Frequency Range	dc to 30 kHz
Accuracy (15°C to 35°C, 90 days with respect to the External Reference, E_{XR}) 16v Range	±(0.01% of program +.0001%$\left(\frac{75}{E_{XR}}\right)$ +100 uV) at dc.
65v Range	±(0.01% of program +.0001%$\left(\frac{75}{E_{XR}}\right)$ +300 uV) at dc.
Programming Resolution (Least significant bit)	
16v Range	$E_{XR} \times 10^{-4}$ volts
65v Range	$E_{XR} \times 4 \times 10^{-4}$ volts
PROGRAMMABLE CURRENT LIMIT (Option –06)	
100 ma Range	±10 mA to ±110 mA in 10 mA increments
1 amp Range	±100 mA to ±1.1 amp in 100 mA increments
Minimum program possible	±10 mA
SPEED	Settles to 0.01% of the programmed change in 100 μsec. A range change does not increase settling time.
OUTPUT STABILITY (Constant load, line and temperature)	
16v Range, 24 hours	±(10 ppm of program + 40 uv)
90 days	±(30 ppm of program + 70 uv)
65v Range, 24 hours	±(10 ppm of program +120 uv)
90 days	±(30 ppm of program +210 uv)
TEMPERATURE COEFFICIENT (35°C to 15°C)	
16v Range	±(10 ppm of program +15 uv) per °C
65v Range	±(10 ppm of program +15 uV) per °C
LOAD REGULATION	An output current change of 1 ampere causes the output voltage to change less than 0.001% of range.
LOAD RECOVERY	The output voltage will settle to within 0.01% of final value in 100 μsec after an output current change of 1 amp.

LINE REGULATION	The output voltage will change less than 0.001% of range for a ±10% change in line voltage.
OUTPUT TERMINALS	HIGH, LOW, HIGH SENSE, LOW SENSE, CHASSIS, GUARD. Terminals located on rear panel. The GUARD terminal can be floated up to 1000 volts above chassis ground.
PROGRAM CONTROL CONNECTOR (See Table 1-3)	A 50 pin connector on rear panel. Mating connector is Amphenol, Blue Ribbon, Part No. 57-30500.
INPUT POWER	115/230 vac ±10%, 48–62 Hz single phase, 200 watts fully loaded.
ENVIRONMENTAL	
Temperature	0°C to 50°C operating; –40°C to 75°C storage.
Relative Humidity	0 to 80%
Shock	20g, 11 millisecond half-sine wave
Vibration	4.5g, 10–55 Hz
Altitude	0 to 10,000 ft - Operating 50,000 ft – Non-operating
SIZE (See Figure 1-1)	5–1/4" high x 17" wide x 19–7/8" (max) deep
ACCESSORIES	
Manual Control Unit	Allows manual checkout, calibration, and control. FLUKE Model A4200.
Rack Mounting Brackets	M05-205-600
Chassis Slides	M00-260-610 (18") M00-280-610 (24")
Mating Connector	Amphenol, Blue Ribbon 57-30500, FLUKE PART NO. 266056.
Extender Card	FLUKE PART NO. 292623

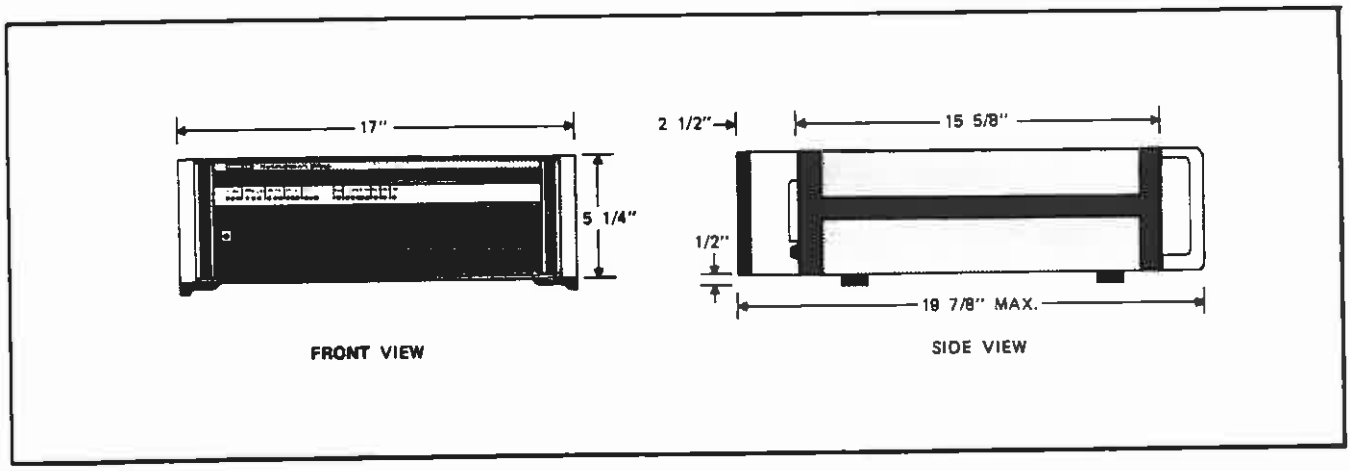


Figure 1-1. OUTLINE DRAWING

Table 1-2. PROGRAMMING INPUT/OUTPUTS

PROGRAM CONTROL	All program control and response lines are compatible with DTL and TTL logic. Programming lines are brought out on the rear panel.
LOGIC LEVELS	Logic "1" = 0 ±.4 vdc or contact closure. Logic "0" = +2 to +5 vdc or open circuit
SIGN	Connector Pin 35. Logic "1" = Negative output voltages
MAGNITUDE	Bit Wt. / Conn. Pin: 2^{13} / 1; 2^{12} / 2; 2^{11} / 3; 2^{10} / 4; 2^{9} / 5; 2^{8} / 6; 2^{7} / 7; 2^{6} / 8; 2^{5} / 9; 2^{4} / 10; 2^{3} / 11; 2^{2} / 12; 2^{1} / 13; 2^{0} / 14. *Two's complement binary coding for negative values is used with the Isolated Control Logic Option –01. Sign and magnitude binary coding is used with the direct coupled control logic Option –04.*
DATA STROBE	Connector pin 33. When using the Isolated Control Logic, a strobe pulse is required to start the digital-to-analog conversion process after a valid command is present. Minimum pulse width is 500 nanoseconds. A negative leading slope (+5V to 0V transition) is required. Upon release of the Data Strobe, the output will go to the programmed value. If the Data Strobe is not used in the Direct Coupled mode, the output will follow any command data perturbations. Logic "1" = "hold" condition.
RANGE	Connector Pin 29; Logic "0" = Low Voltage Range, Logic "1" = High Voltage Range.
EXTERNAL REFERENCE	Connector Pin 36; Logic "0" = Internal DC Reference, Logic "1" = External Reference.
STANDBY	Connector Pin 34; Logic "0" = Operate Mode, Logic "1" = Standby; Output is approximately 1% of programmed level.
CURRENT LIMIT	Connector Pin 42: Function Range, Logic "1" 1 Amp, Logic "0" 100 mA. Connector Pin 43: Magnitude, 80% of Range, Logic "0" 0. Connector Pin 44: Magnitude, 40% of Range, Logic "0" 0. Connector Pin 45: Magnitude, 20% of Range, Logic "0" 0. Connector Pin 46: Magnitude, 10% of Range, Logic "0" 0. All "0"s = 10% of range
RESPONSE SIGNALS	
CURRENT LIMIT FLAG	Connector Pin 49; Logic "1" represents a current overload condition.
READY/NOT READY FLAG	Connector Pin 37; Logic "0" = "Ready" condition; the output is within 0.01% of the programmed increment for a resistive load. Logic "1" = "Not Ready" condition; the power source is in the process of settling to the programmed value.
POWER CONNECTIONS	Connector Pin 25; An internal, isolated power supply furnished +5 vdc, current limited by 2.7 ohms, for use by the external system interface logic.
LOGIC GROUND	Connector Pins 17 thru 24; It is recommended that a large ground strap be used between the interface logic and the power source to reduce the digital programming noise on the system ground.

List of Illustrations

(continued on page iv)

LIST OF ILLUSTRATIONS, *continued*

List of Tables

Section 2
Operating Instructions

2-1. INTRODUCTION

2-2. This section contains information regarding installation and operation of the Model 4265A. It is recommended that the contents of this section be thoroughly read and understood before any attempt is made to operate this power source. Should any difficulties be encountered during operation, please contact your nearest John Fluke Sales Representative or the John Fluke Mfg. Co., Inc., P.O. Box 7428, Seattle, Washington 98133, telephone (206) 774-2211. A list of Sales Representatives is located at the rear of this manual.

2-3. SHIPPING INFORMATION

2-4. The Model 4265A was packaged and shipped in a foam packed cardboard carton. Upon receipt, a thorough inspection should be performed to reveal any damage in transient. Special instructions for inspection and claims are included in the carton.

2-5. If reshipment of this power source is necessary, the original container should be used. If the original container is not available, a new one can be obtained from the John Fluke Mfg. Co., Inc. Please reference the Model number when requesting a new shipping container.

2-6. INPUT POWER

2-7. This power source can be operated from either a 115 or 230 vac, 48 to 62 Hz, power line. A decal on the rear panel indicates which power line input is required. If it becomes necessary to change from one power line voltage to the other, proceed as follows:

a. Disconnect the power cord from the rear panel of the power source.

b. Remove the top dust cover and inner cover.

c. Locate the Power Supply Assembly and 115/230 slide switch shown in Figure 2-1.

d. Set the slide switch to the desired line voltage position. Positions are labeled on the printed circuit board.

e. Replace the inner cover and top dust cover.

f. Install the following rated value fuse in the rear panel fuse holder.

115 VAC	230 VAC
2A, AGC	1A, AGC

g. Reconnect the power cord at the rear panel and then energize the power source with the toggle switch on the rear panel. The POWER lamp on the front panel should illuminate.

2-8. RACK INSTALLATION

2-9. The power source is designed for bench-top use or for installation in a 19 inch equipment rack using the Accessory Rack Mounting Kit shown in Figure 2-2. Accessory chassis slides can also be installed to better facilitate rack installation. Information regarding installation of these Ac-

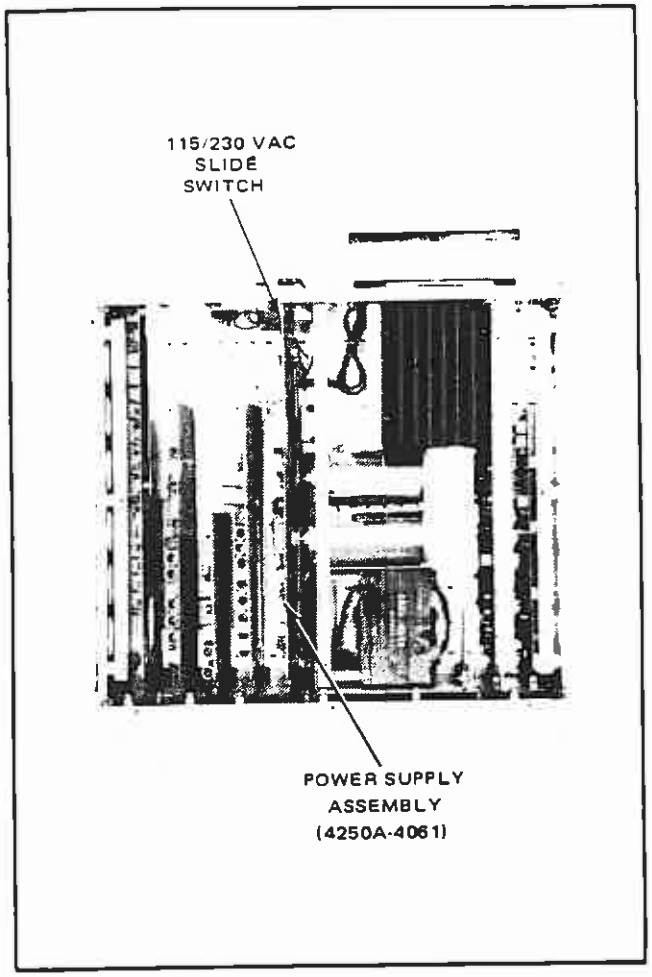


Figure 2-1. 115/230 VAC POWER CONVERSION

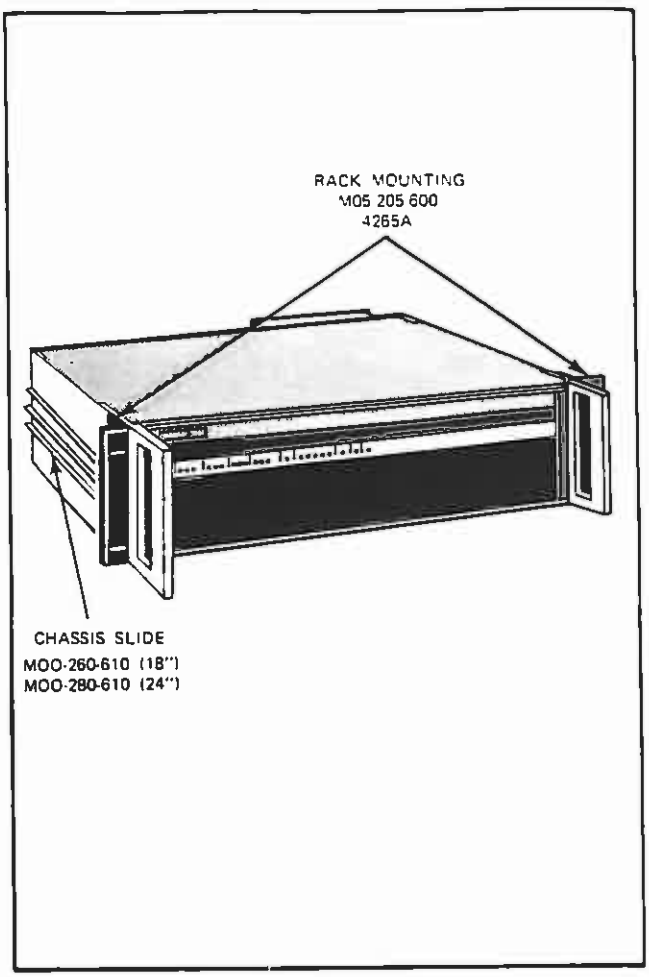


Figure 2-2. ACCESSORY RACK MOUNTING KITS

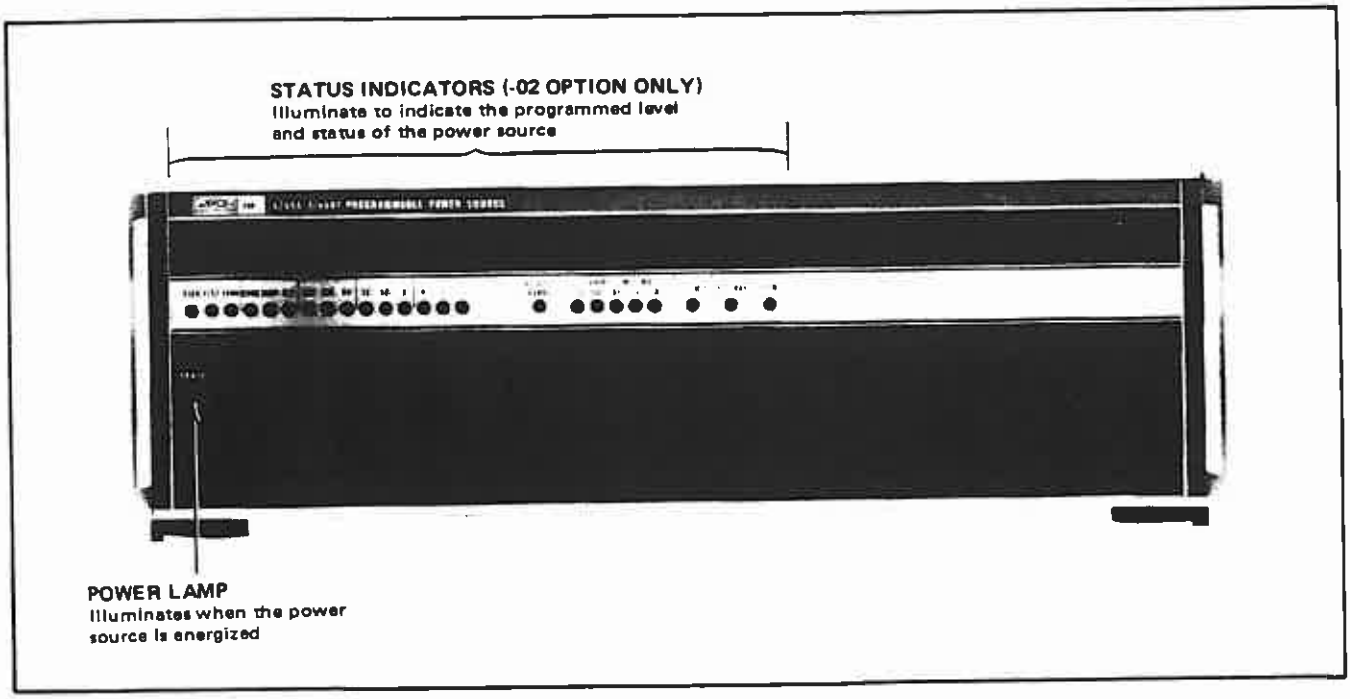


Figure 2-3. OPERATING FEATURES (Sheet 1 of 2)

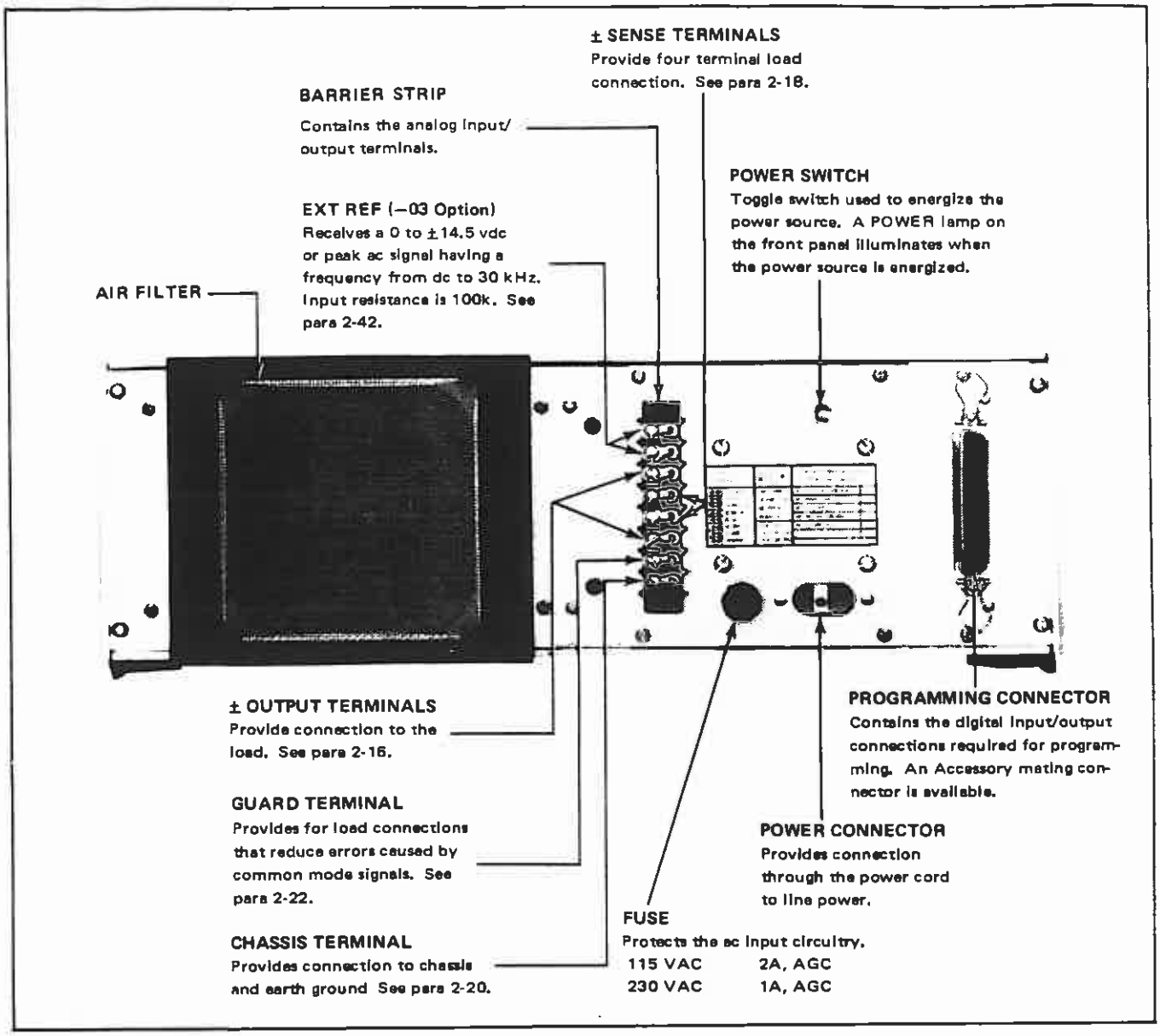


Figure 2-3. OPERATING FEATURES (Sheet 2 of 2)

cessories is given in the Section 6, Rack Installation subsection.

2-10. OPERATING FEATURES

2-11. The location and function of all connectors and indicators is given in Figure 2-3.

2-12. OPERATING NOTES

2-13. The following paragraphs describe various conditions which should be considered before operating the Model 4265A.

2-14. AC Line Connection

2-15. The input power cord plug is a three prong, polarized connection. This plug allows connection to either a 115 or 230 vac, 48 to 62 Hz, power line (see Input Power, paragraph 2-6), while at the same time connects the power source chassis to earth ground. Always ensure that the round pin is connected to a high quality earth ground. The power source is energized through a toggle switch on the rear panel.

2-16. Load Connections

2-17. An eight terminal barrier strip, located on the rear panel, serves as an analog input/output connector for the power source. The ± power output terminals (OUTPUT HI and LO) provide connection to the load. The ± sense ter-

minals (SENSE HI and LO) are provided to allow remote sensing at the load. The sense terminals are bussed through jumpers installed at the factory to the output terminals. If remote sensing is not required, the load is connected to the respective ± output terminals and the sensing busses are not removed. If remote sensing is required, the busses must be removed and separate sense lines provided between the sense terminals and the load. In either case, NEVER operate the power source with the sense terminals disconnected. The CHASSIS terminal is connected directly to the chassis and allows grounding of the load through the input power cord, if desired. The GUARD terminals allows load connections that can greatly reduce errors caused by common mode signals. This guard connection should always be used if optimum noise free performance is to be achieved.

2-18. Remote Sensing

2-19. When a load is connected to the OUTPUT terminals, the I-R drop across the output power leads may be excessive in some applications. If the rated accuracy of the power supply is required at the load, remote sensing must be used. For this reason, SENSE terminals are provided to allow the power supply output to be sensed directly at the load, thus compensating for any I-R drop in the output power leads. Figure 2-4 shows an example of remote sensing load connections.

NOTE!

*The two jumpers on the barrier strip which bus ± sense to ± output must be removed for remote sensing. When remote sensing, always use a twisted pair of insulated wire from the output and sense terminals to the load. A maximum of 0.35 volts (at 25°C, decreasing 0.002 volts per degree C at higher temperatures) is allowable between either **OUTPUT** terminal and its corresponding **SENSE** terminal. The leads between the OUTPUT and SENSE terminals and the load must be large enough to carry the load current of up to 1 ampere and the sense current of 1 ma without exceeding this voltage.*

2-20. Ground Connections

2-21. A CHASSIS terminal is provided at the rear panel. This terminal is directly connected to the chassis of the power source and earth ground through the round pin on the input power plug. If grounding of the load is desired, this terminal provides a convenient connection to earth ground. When a guarded output (explained in paragraph 2-22) is not desired, this terminal should be connected to the GUARD terminal.

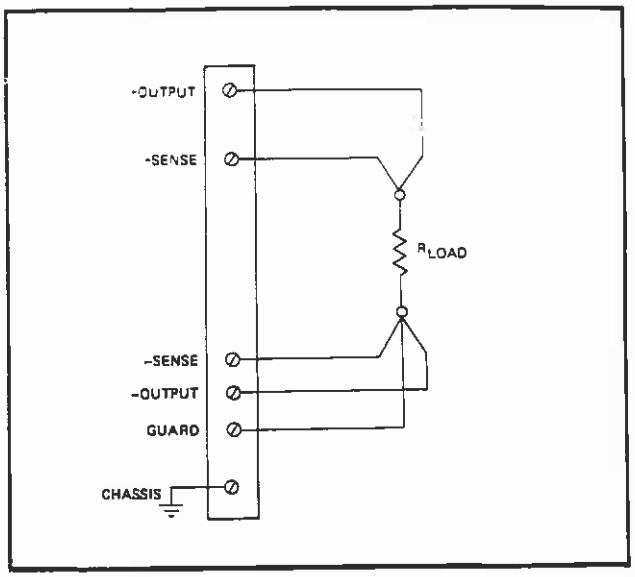


Figure 2-4. REMOTE SENSING CONNECTIONS

2-22. Guard Connections

2-23. The power source is equipped with a guard shield that isolates its internal circuitry from the chassis and ground. A GUARD terminal at the rear panel is connected to this shield and allows load connections that greatly reduce errors caused by common mode signals. The guard may be driven to a maximum of 1000 volts above chassis ground. Figure 2-5 shows a simplified diagram of a guarded load connection.

2-24. PROGRAMMING INFORMATION

2-25. Digital control of all functions except POWER ON is accomplished through a 50 pin Amphenol, Blue Ribbon connector on the rear panel. The power source is energized through a toggle switch on the rear panel. Interface between the programming equipment and the power source requires an Amphenol, Blue Ribbon 57-30500 mating connector. This mating connector is available as an accessory for the power source. It can be obtained from FLUKE under PART NO. 266056. Installation information reguarding this connector is located in Section 6 . Table 2-1 lists and describes each terminal on the Programming Connector.

2-26. Programming input requirements are compatible with either DTL or TTL logic levels. Logic "0" is +2.0 to 5.0 vdc or open circuit to logic ground. Logic "1" is +0.4 vdc or short circuit to logic ground. Logic ground is

available at pins 17 through 24 of the programming connector. Shorting these lines to the appropriate pins of the programming connector using contact closures also allows control of the power source. The internal +5 vdc output, current limited by 2.7 ohms, is available at pin 25 for use by the external programming logic.

2-27. Standby

2-28. The STANDBY mode can be programmed by applying a Logic "1" to pin 34 of the Programming Connector. When this condition exists, the output voltage of the power source will be less than 1% of the programmed value. Application of a Logic "0" at this pin returns the output voltage to the programmed level.

2-29. Range/Output Magnitude/Polarity

2-30. Two voltage ranges are available; ±16 volts and ±65 volts. The RANGE is programmed by a single line input at pin 29 of the Programming Connector. A Logic "0" applied to this pin will program the ±16 volt range, and a Logic "1" will program the ±65 volt range. The power supply is capable of an output of ±66v minimum at 1 ampere.

2-31. The magnitude of the output voltage is programmed with binary coded inputs at pins 1 through 14 of the Programming Connector. When the 16 volt range is called, resolution is in 1 mv steps. In the 65 volt range, resolution is in 4 mv steps and the programmed output voltage is four times that of the binary input. Upon installation of a jumper in the Preamplifier (4265A-4051), the bit weight can be changed to give a MSB of 8.000v in the 16 volt range and 32.000v in the 65 volt range.

2-32. Polarity of the output is controlled by a single binary input (SIGN) at pin 35 of the Programming Connector. A Logic "0" will produce a positive output, and Logic "1" will produce a negative output. When the Isolated Control Logic (–01 Option) is installed, Two's complement coding is required for negative outputs. Table 2-2 shows a comparison between binary and Two's complement coding.

2-33. Data Strobe

2-34. The DATA STROBE shown in Figure 2-6 is required to initiate the transfer of the data present at the programming inputs to the internal memory of the Isolated Control Logic (–01 Option). The DATA STROBE is applied to pin 33 of the Programming Connector. Upon its negative

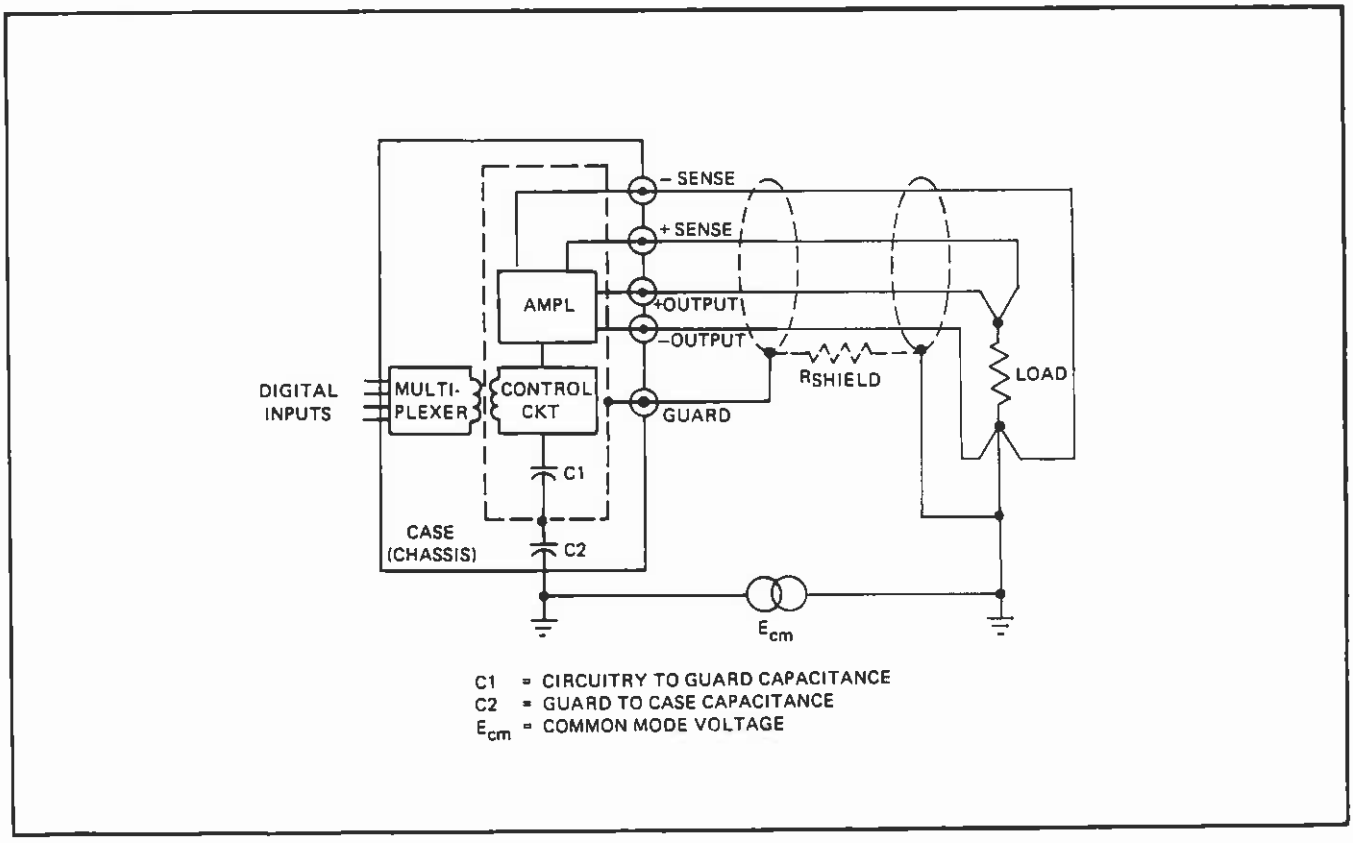


Figure 2-5. GUARDED LOAD CONNECTION

Table 2-1. PROGRAMMING INPUT/OUTPUTS

LOGIC "0" = +2 to +5 vdc or open circuit

LOGIC "1" = 0 + 0.4 vdc or short circuit to LOGIC GRD

PIN NO.	FUNCTION		
	CODE = LOGIC "1"	16V RANGE (1 mv steps)	65V RANGE (4 mv steps)
1	8192	8192	32768
2	4096	4096	16384
3	2048	2048	8192
4	1024	1024	4096
5	512	512	2048
6	256	256	1024
7	128	128	512
8	64	64	256
9	32	32	128
10	16	16	64
11	8	8	32
12	4	4	16
13	2	2	8
14	1	1	4
15, 16	NOT USED		
17, 18, 19, 20, 21, 22, 23, 24	LOGIC GRD		
25	LOGIC PWR (+5 vdc current limited by 2.7 ohms)		
26, 27, 28	NOT USED		
29	VOLTAGE RANGE: LOGIC "0" = 16V LOGIC "1" = 65V		
30, 31, 32	NOT USED		

PIN NO.	FUNCTION
33	DATA STROBE (See Figure 2-6 and 2-7) INITIATES DIGITAL TO ANALOG CONVERSION
34	STANDBY/OPERATE: LOGIC "0" = OPERATE LOGIC "1" = STANDBY
35	SIGN: LOGIC "0" = POSITIVE OUTPUT LOGIC "1" = NEGATIVE OUTPUT
36	EXTERNAL REFERENCE (–03 Option): LOGIC "0" = INTERNAL REFERENCE LOGIC "1" = EXTERNAL REFERENCE
37	READY/NOT READY FLAG: LOGIC "0" = READY LOGIC "1" = NOT READY
38, 39, 40, 41	NOT USED
42	CURRENT LIMIT RANGE (–06 Option): LOGIC "0" = 100 MA LOGIC "1" = 1 AMP
43	LOGIC "1" = 80%
44	LOGIC "1" = 40%
45	LOGIC "1" = 20%
46	LOGIC "1" = 10% CURRENT LIMIT % RANGE (–06 Option) *NOTE: All "0"'s = 10% of Range*
47, 48	NOT USED
49	CURRENT LIMIT FLAG: LOGIC "0" = NORMAL LOGIC "1" = OVERLOAD
50	NOT USED

Table 2-2. BINARY AND TWO'S COMPLEMENT CODING (16V RANGE)

OUTPUT VOLTAGE	BINARY		OUTPUT VOLTAGE	TWO'S COMPLEMENT	
	Sign	Code		Sign	Code
Ov	0	00000000000000	Ov	1	00000000000000 (not valid)
+1 mv	0	00000000000001	–1 mv	1	11111111111111
+8.192	0	10000000000000	–8.192	1	10000000000000
+16.383	0	11111111111111	–16.383	1	00000000000001

transition, program data transfer begins. At the same time, two pulses are generated; 15 μsec and 100 μsec. The 15 μsec pulse holds the power supply output at its previously programmed level while new data is transferred into memory and allowed to settle. At the end of the 15 μsec pulse the power source is allowed to respond to the new program data. The 100 μsec pulse provides a READY/NOT READY output that indicates the power source has had time to respond to new program data and the output to be within ±0.01% of the programmed change for a resistive load. Program data must be present and settled for a minimum of 2.4 μsec after the negative transition of the DATA STROBE.

NOTE!

When the power supply is initially turned on or if a power interruption occurs, the power supply is programmed to zero volts, where it will remain until new data is transferred.

2-35. When the Direct Coupled Logic (–04 Option) is installed, the DATA STROBE shown in Figure 2-7 is used to hold the output voltage constant while programming data is changed. However, the period of the DATA STROBE must match the program change interval. If this is not done, the output will follow any program changes, which is normal for direct programming. The 100 μsec READY/NOT READY FLAG begins at the end of positive transition of the DATA STROBE and serves to indicate the source has had time to respond to new program data and be within ±0.01% of the programmed change for a resistive load.

2-36. Flag Outputs

2-37. Two flag outputs are provided to indicate when a current overload exists, and when the output voltage has had time to settle. A current OVERLOAD is indicated by a Logic "1" at pin 49 of the Programming Connector. Normal operation is indicated by a Logic "0". Output settling time is indicated by a READY/NOT READY FLAG at pin 37. Logic "0" is the READY condition and indicates that the output voltage has had time to settle to within 0.01% of the programmed change for a resistive load. A Logic "1" indicates a NOT READY condition.

2-38. The OVERLOAD FLAG and the NOT READY FLAG will both be activated when a sink or source current overload occurs. After the overload is removed, the OVERLOAD FLAG will return to normal but the NOT READY FLAG will remain for 100 μsec to allow for output settling time. Figure 2-6 and 2-7 show the timing relations of these flags. If the Programmable Current Limiting (–06 Option) is installed, the OVERLOAD FLAG will also be activated when current limiting occurs.

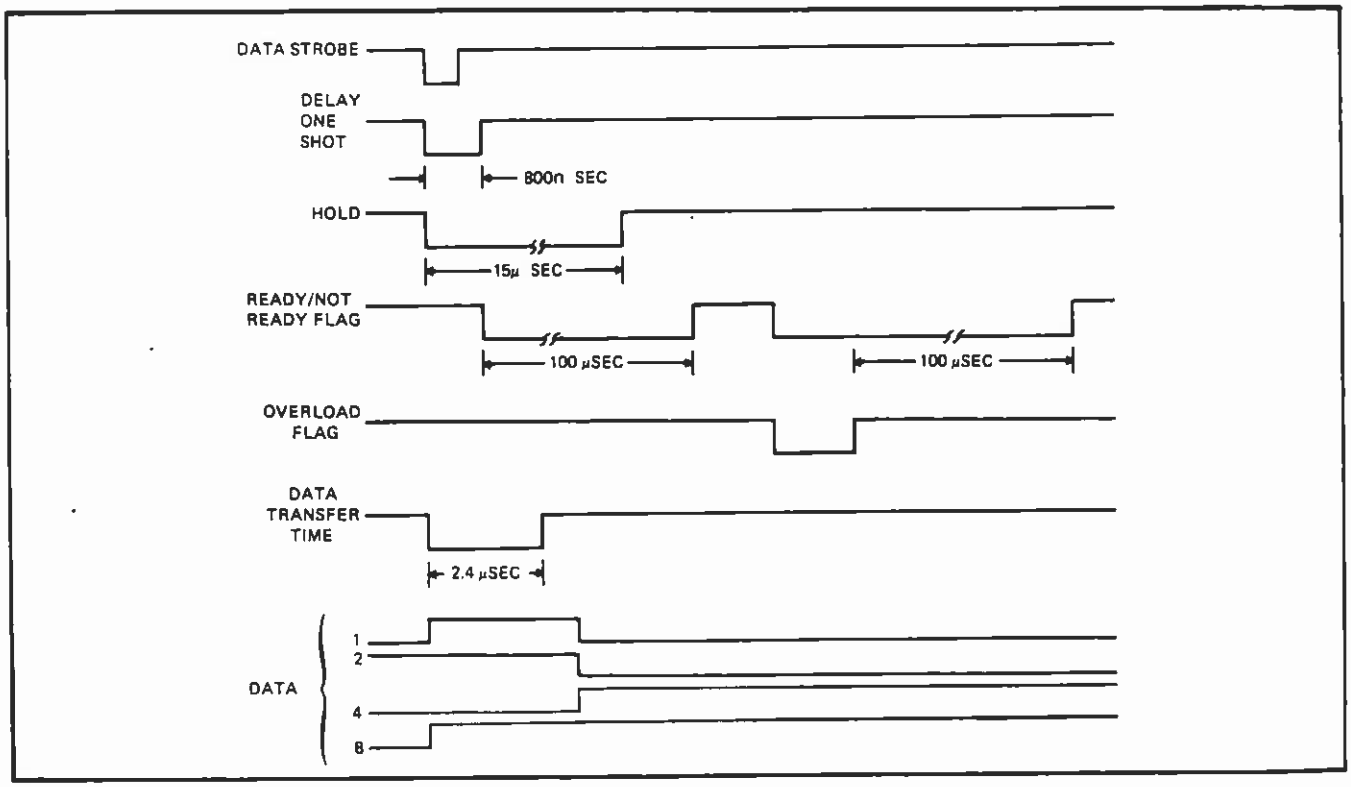


Figure 2-6. ISOLATED CONTROL LOGIC TIMING (–01 OPTION)

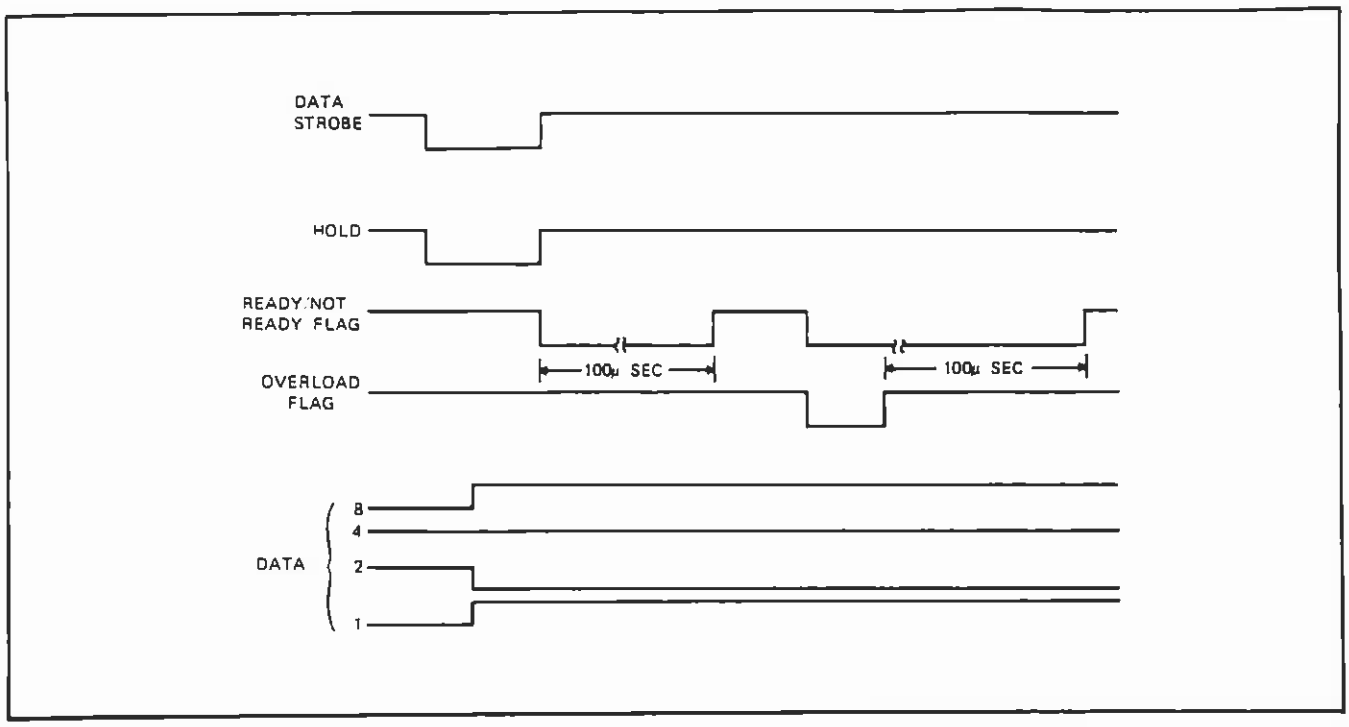


Figure 2-7. DIRECT CONTROL LOGIC TIMING (–04 OPTION)

2-39. Programmable Current Limiting

2-40. When the Programmable Current Limiter (–06 Option) is installed, two ranges of current limiting are available; ±1.0 amp and ±100 ma. The CURRENT RANGE is programmed by a single binary input at pin 42 of the Programming Connector. A Logic "0" applied to this pin programs the 100 ma range and a Logic "1" programs the 1.0 amp range.

2-41. The magnitude of the output current is programmed by applying binary coding to pins 43 through 46 of the Programming Connector. Current magnitude programming is in increments of 10% of the programmed range. If all current magnitude inputs are programmed to Logic "0", the current limit is still 10% of the programmed range. The maximum current limit that can be programmed is 110% of the programmed range. When current limiting occurs, the OVERLOAD FLAG changes from Logic "0" to Logic "1" as described in paragraph 2-38.

NOTE!

A sink capability greater than the programmed current limit value cannot be realized.

2-42. External Reference

2-43. When the External Reference (–03 Option) is installed, a single programming bit is used to remove the internal 10 vdc reference from the D-to-A ladder network and switch in an external signal source to replace it. The output accuracy and stability of the power source, however, is then relative to the accuracy and stability of the external signal source.

2-44. The external reference may be any dc or ac signal with an amplitude between 0 and ±14.5 vdc or peak ac (volts rms x 1.414) and have a frequency between dc and 30 kHz. It is applied to the ± EXT REF terminals located on the rear panel barrier strip. The input impedance at these terminals is 100k ohms in parallel with 70 pf. The EXT REF is programmed by applying a Logic "1" to pin 36 of the Programming Connector. It should be noted that the polarity of the output will be the same as the EXT REF regardless of the SIGN (polarity) program. For this reason, only a positive binary magnitude code should be used when the EXT REF is an ac signal.

2-45. Programming the magnitude of the output voltage with a ±10 volt EXT REF is accomplished by the same method used for programming with the internal reference voltage. (See paragraph 2-31.) However, if the EXT REF is not exactly ±10 volts, the magnitude of the programming word required to obtain a specified output voltage must be calculated as follows:

MPW = Magnitude of the programming word.

E_{OUT} = Output (vdc)

EXT REF = External Reference voltage (vdc or peak ac)

16 volt range: $E_{OUT} = (MPW \times 10^{-4})(EXT\ REF)$ therefore:

$$MPW = \frac{E_{OUT}}{EXT\ REF} \times 10^{4}$$

Programming resolution = EXT REF x 10^{-4}

---

65 Volt range: $E_{OUT} = (4\ MPW \times 10^{-4})(EXT\ REF)$ therefore:

$$MPW = \frac{E_{OUT}}{4\ (EXT\ REF)} \times 10^{4}$$

Programming resolution = 4 (EXT REF) x 10^{-4}

NOTE: $E_{OUT} \leq 66$

It should be noted that the rated output of the power supply is ±66v minimum at 1 ampere. Higher voltage output is obtainable depending on line voltage and output current, i.e. ±85v typical at 115 vac line and no load. It therefore becomes obvious that when using the 65 volt range, the programming word can easily exceed the output capability of the power source. The following example, using previously shown formula for the 65 volt range, will clearly illustrate this.

Example:

Find: E_{OUT}

Given: **EXT REF** = +14.5 vdc, MPW = 16.383, **Range** = 65 volt

$E_{OUT} = (4\ MPW \times 10^{-4})(EXT\ REF)$

$(4 \times 16.383 \times 10^{-4})(14.5)$

$(6.5532)(14.5)$

E_{OUT} = 95.0214 vdc

E_{OUT} in this example greatly exceeds the 66 volt output capability of the power supply. To avoid this situation always calculate MPW with E_{OUT} VO ≤ 66.

2-46. Front Panel Indicators

2-47. When the Front Panel Display (–02 Option) is installed, status lamps (light emitting diodes) are provided on the front panel. These lamps indicate the programmed output voltage level, output polarity, current overload, current limit level, external reference, and standby status of the internal register. None of these lamps are provided when the BLANK FRONT PANEL (–05 Option) is installed. A POWER lamp is included with either option to indicate that the power source is energized.

2-48. Dynamic Characteristics

2-49. The power source output can be changed quite rapidly with high speed programming information. However, a 100 μsec period must be allowed before the output has settled to its stated accuracy for a resistive load.

2-50. When an external signal is used as the reference for the power source, the output accuracy is dependent upon the characterisitics of the external signal. If a dc voltage is used, the output accuracy is related to the accuracy and stability of the external voltage. However, if an ac signal is used, the output accuracy is not only dependent upon the external signal stability, but also its frequency. Typical examples of accuracy versus frequency are shown in Figures 2-8 through 2-11.

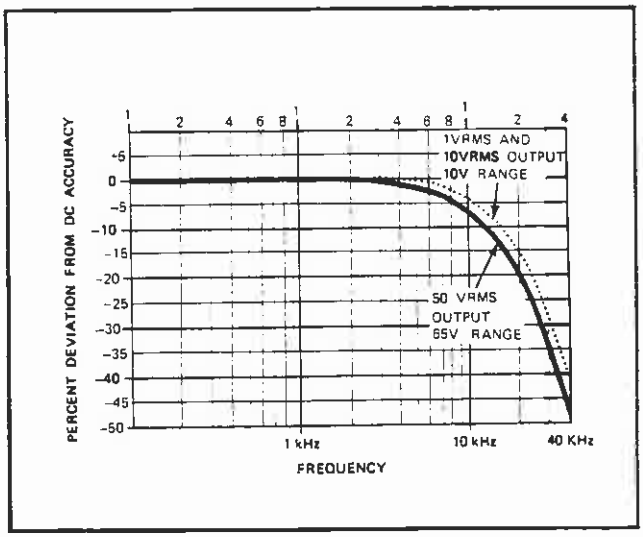


Figure 2-8. ACCURACY VERSUS EXTERNAL REFERENCE FREQUENCY

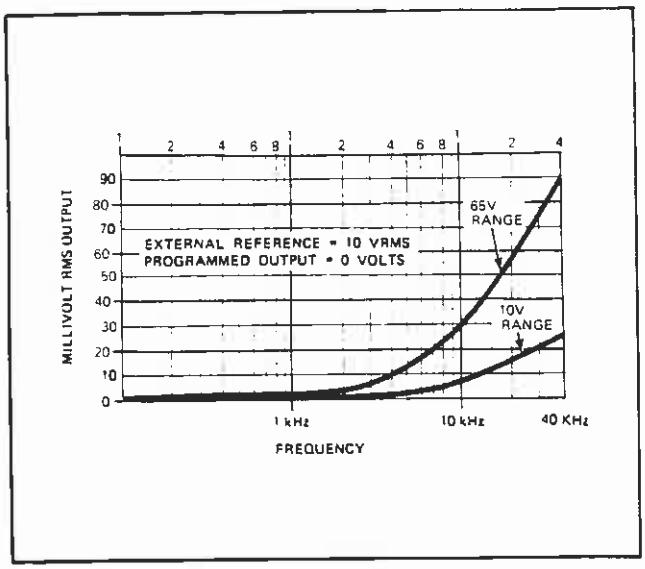


Figure 2-9. AC EXTERNAL REFERENCE FEED-THROUGH VERSUS FREQUENCY (OV OUTPUT)

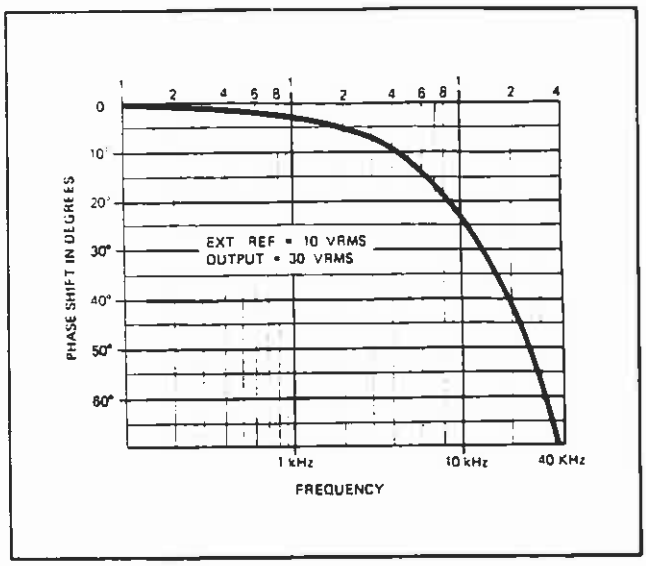


Figure 2-10. AC EXTERNAL REFERENCE PHASE SHIFT VERSUS FREQUENCY

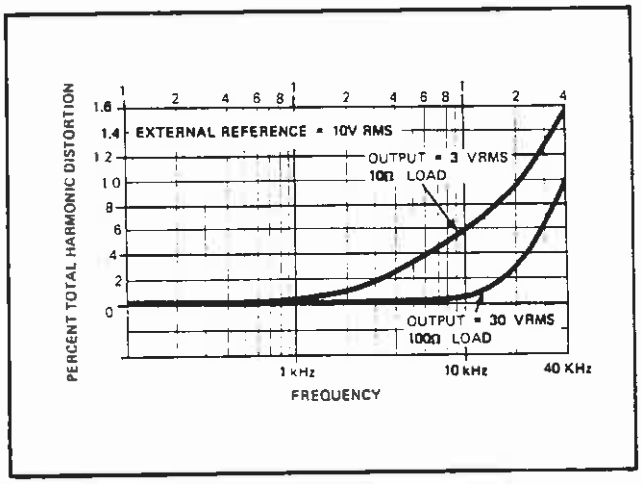


Figure 2-11. AC EXTERNAL REFERENCE HARMONIC DISTORTION VERSUS FREQUENCY

Section 3

Theory of Operation

3-1. INTRODUCTION

3-2. This section contains the theory of operation for the Model 4265A. The information is arranged under headings of "FUNDAMENTAL CIRCUIT DESCRIPTIONS, BLOCK DIAGRAM ANALYSIS, and CIRCUIT DESCRIPTIONS." An equivalent circuit of the power source is shown in Figure 3-1. Figure 3-2 is a simplified block diagram that includes all options.

3-3. FUNDAMENTAL CIRCUIT DESCRIPTION

3-4. The Model 4265A converts a digital program word into a representative dc output voltage. Basically, the circuitry consists of a high gain operational amplifier shown in Figure 3-1. Digital to analog conversion is done using a ladder network driven by a bi-polar reference voltage. The differential amplifier then produces an output voltage (Vo) that is maintained by the current through R_f as determined by the ratio of V_{REF} over R_o $\left(\frac{V_{REF}}{R_o}\right)$

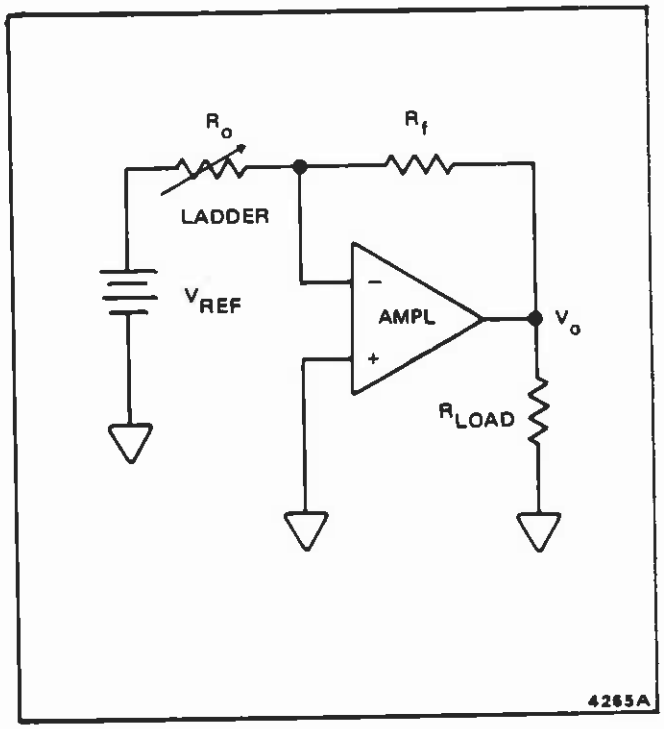


Figure 3-1. POWER SOURCE EQUIVALENT CIRCUIT

3-5. BLOCK DIAGRAM ANALYSIS

3-6. The following paragraphs describe the major circuit functions of the Model 4265A. A block diagram of the power source, including all options, is shown in Figure 3-2.

3-7. One of two A6 Logic assemblies receive and process the digital inputs. The Isolated Control Logic (−01 Option) provides isolation and storage of the digital inputs. A STROBE input is required for any data transfer. The Direct Coupled Control Logic (−04 Option) provides only level shifting of the inputs. Both assemblies provide READY/NOT READY and CURRENT LIMIT FLAG outputs. Internal commands from the A6 LOGIC control polarity, range, magnitude, sample and hold, and current limiting of the output. These commands (except sample and hold) are also applied to the A7 Display where, if the −02 Option is installed, visual status is provided on the front panel.

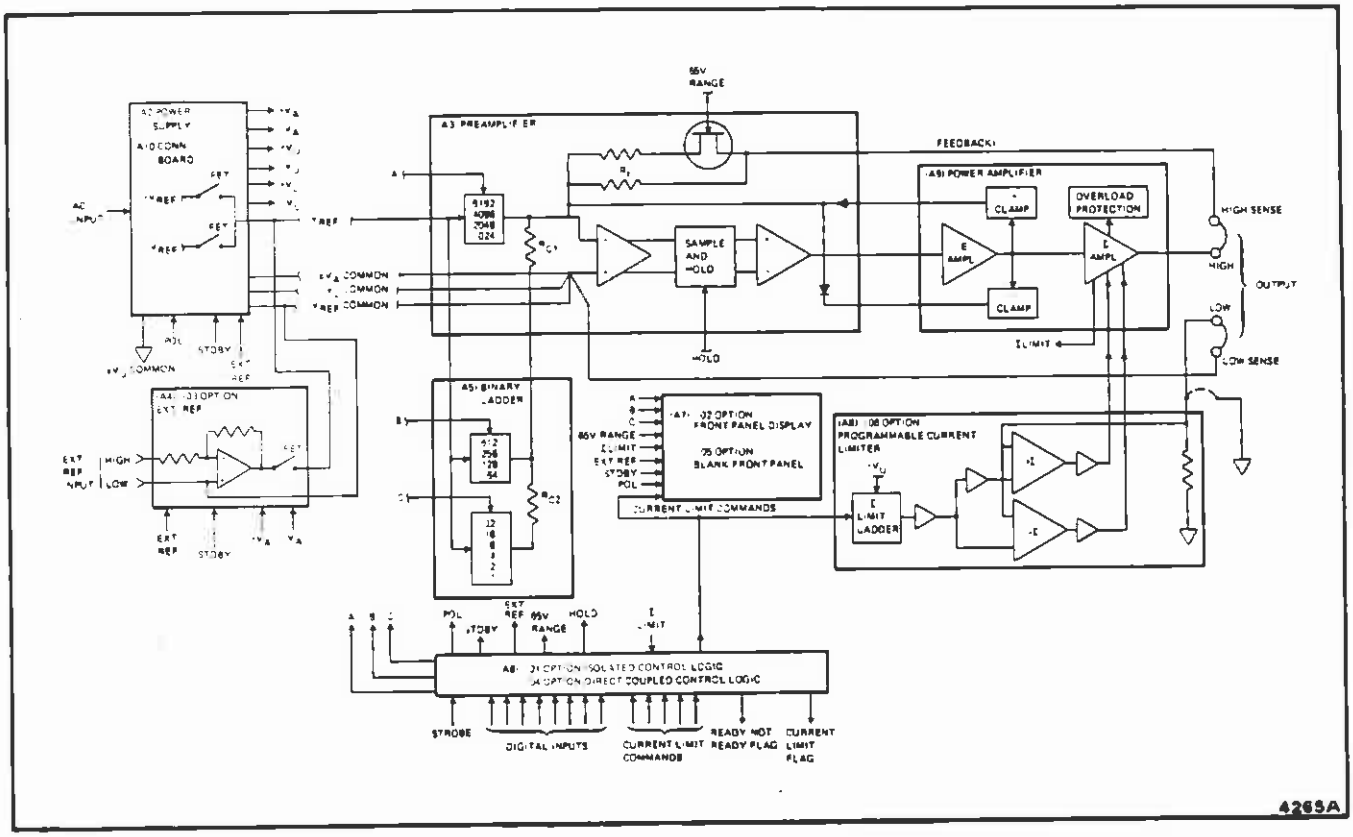


Figure 3-2. MODEL 4265A BLOCK DIAGRAM

3-8. All operating voltages as well as the internal reference voltage (V_{REF}) are produced in the A2 Power Supply and the A10 Connector Board. Commands from the A6 Logic determine the polarity of V_{REF} applied to V_{REF} bus line. A +POL command produces a $-V_{REF}$ and a −POL command a $+V_{REF}$. Presence of either or both EXT REF and STDBY commands disables the internal V_{REF}.

3-9. The A4 External Reference (−03 Option) processes the external reference input voltage. The magnitude of this voltage can be from 0 to ±14.5V dc or peak ac and have a frequency from dc to 30 kHz. Presence of an EXT REF command disables the previously described internal V_{REF} and applies the output of the A4 External Reference to the V_{REF} bus line. If a STDBY command exists, the external V_{REF} is disabled.

3-10. Binary ladder networks in the A3 Preamplifier and A5 Binary Ladder scale the selected internal or external V_{REF} to a level determined by the A, B, and C commands. This scaled voltage is then inverted and amplified by voltage and power amplifiers in the A3 Preamplifier and A9 Power Amplifier. Current through R_f in the A3 Preamplifier maintains a proportional output voltage dependent upon the value of R_f, ladder, and polarity of V_{REF}. In the 16V range, the total parallel value of R_f in combination with an internal V_{REF} estab-

lishes an output in millivolts directly proportional to the digital input word. The value of R_f is increased by four times in the 65V range by disconnection of one of the R_f resistors. Subsequently, outputs in the 65V range are four times the digital input word. When the external V_{REF} is selected, the output is proportional to the combined effects of the external reference magnitude and the digital input word. Actual output is determined as follows:

16V Range: Eout = MPW x 10^{-4}) (EXT REF)
65V Range: Eout = (4MPW x 10^{-4}) (EXT REF)
Where: MPW = Magnitude of digital input word
EXT REF = External reference voltage. (V dc or peak ac):

3-11. Programming changes are prevented from appearing at the output until the entire digital input word is stored. This is provided through the sample and hold circuit in the A3 Preamplifier. Presence of a STROBE input to the A6 Logic produces a HOLD command which activates the sample and hold circuit. The sample and hold disconnects and stores the last input to the voltage amplifier, thus providing a memory condition for the duration of the HOLD command. The HOLD command has a duration of 15 μsec when the A6 Isolated Control Logic (−01 Option) is installed. Duration of the HOLD command is proportional to the STROBE input when the A6 Direct Coupled Control Logic (−04 Option) is installed.

3-12. Overload protection circuitry in the A9 Power Amplifier automatically limits the maximum output current to 1.2A. Whenever a current limit occurs, an I LIMIT command is applied to the A6 Logic which then produces a CURRENT LIMIT FLAG output. Current limiting at less than 1.2A is also possible using the A8 Programmable Current Limiter (−06 Option) described later. Clamp circuits in the A9 Power Amplifier limit voltage transients at the output during a current limit condition when the load is disconnected.

3-13. Current limiting at less than 1.2A is provided upon installation of the A8 Programmable Current Limiter (−06 Option). Maximum bipolar output current can be limited to a level between 10 ma and 1.1 ampere in 10 percent steps on two separate ranges. In the event the output current is clamped at that level by action of the A8 Programmable Current Limiter. During periods of current limiting, an I LIMIT command is generated in the A9 Power Amplifier and is applied to the A6 Control Logic and to the A7 Front Panel. The I LIMIT command applied to the A6 Control Logic produces a CURRENT LIMIT FLAG at pin 49 of the Programming Connector. The I LIMIT command applied to the A7 Front Panel illuminates the I LIMIT indicator on the front panel if the −02 Option is installed.

3-14. CIRCUIT DESCRIPTIONS

3-15. The following paragraphs describe the circuitry in the power source. Each description is keyed to a schematic diagram located at the rear of the manual.

3-16. A2 Power Supply and A10 Connector Board (Schematic No. 4250A-1061 and 4250A-1012)

3-17. All operating voltages, as well as the internal reference voltage upon which the power source accuracy and stability relies, are produced in the A2 and A10 assemblies. Designations and nominal magnitudes of each voltage is given in Table 3-1.

Table 3-1. OPERATING VOLTAGES

DESIGNATION	VOLTAGE (VDC)
$+V_L$	+5V
$-V_L$	−5V
$\pm V_U$	±104V [1]
$\pm V_A$	+23.4V, −25.1V
V_{REF}	±10V

[1] Approximate (at 115V line voltage, no load)

3-18. INPUT POWER. AC line power at J1 is applied to the primary of T1 through POWER switch S2 and the 115/230 switch S1. The primary of T1 consists of two windings which allow operation from either a 115 or 230V ac line. S1 provides a parallel primary winding connection for 115V ac line operation. A series connection is provided for 230V ac line operation. AC power for the blower M1 is provided from one of the primary windings of T1. The four secondary windings of T1 supply ac voltages to associated power supplies.

3-19. $+V_L$ SUPPLY. The $+V_L$ Supply, composed of CR19 and Q21 through Q24, produces a regulated +5V dc for use by the A6 Logic and external programming equipment. Diode bridge CR19 rectifies the secondary voltage of T1 and supplies the series regulator of Q21 through Q24 with a dc voltage. C16 filters the voltage applied to the regulator. Q22 functions as a constant current source, supplying base drive to Q23. The resulting +5V output

of the regulator is developed across CR23 and R54 which supplies a sample of the output voltage to the base of Q24. The conduction of Q24 will limit the base drive to Q21 and Q23 producing a regulated +5V output. This supply is completely isolated from all other supplies in the instrument and is electrically external of the guard. All other supplies are electrically inside the guard.

3-20. $-V_L$ SUPPLY. The $-V_L$ Supply composed of CR14 and Q16 through Q18 produces the regulated −5V dc required to operate the internal logic circuits. Diode bridge CR14 rectifies the secondary voltage of T1 and supplies the series regulator of Q16 through Q18 with a dc voltage. C13 filters the rectified voltage. The base drive for Q18 and Q17 is derived from the $+V_A$ Supply through R44. Reference voltage for the base of Q18 is derived from the $-V_A$ Supply through the divider consisting of R46 and R47. Any variation in the −5V output is then sensed by Q18, which controls the base drive to A17 and thus Q16, producing a regulated −5V dc output.

3-21. $\pm V_A$ SUPPLY. The $\pm V_A$ Supply produces the regulated +23.4 and −25.1V dc operating voltages that are used to provide power for most analog circuitry. Diode bridge CR4 rectifies the tapped secondary voltage of T1 and supplies positive and negative voltages for the respective $\pm V_A$ regulators. C7 and C8 filter these rectified voltages.

3-22. The $+V_A$ regulator consists of Q12, Q13 and A4. Reference voltage for this regulator is derived from A2 in the V_{REF} supply and is applied to the non-inverting input of A4. The inverting input of A4 receives a sample of the output voltage from the divider, R36 and R37. Any variations in the $+V_A$ output are thus sensed by A4, which controls the base drive to Q12, producing a regulated +23.4V dc output. Q13 together with R33 function to limit the maximum output current of this supply to 125 ma. Should the current through R33 exceed 125 ma, the voltage across R33 will turn on Q13 whick limits the base current to Q12.

3-23. The $-V_A$ regulator consists of Q14, Q15, and A5. R40 and the $+V_A$ supply establish the reference current for the feedback resistor R41. A5 supplies the base drive required by Q15 to maintain the regulated output of −25.1V dc. Q14 and R39 limit the output current in a similiar manner to Q13 and R33 described previously.

3-24. $\pm V_U$ SUPPLY. The $\pm V_U$ Supply produces unregulated ±104V dc operating voltage for the A9 Power Amplifier. Diodes CR1 through CR4 are connected as two full-wave rectifiers to produce $\pm V_U$ operating voltages from the secondary of T1. C1 and C2 filter the resulting outputs. R1 and R2 function as discharge resistors for C1 and C2, respectively.

3-25. V_{REF} SUPPLY. The V_{REF} Supply produces an extremely stable ±10V dc reference upon which the accuracy and stability of the power source is based. Circuitry of this supply consists of a stable reference amplifier A2, a differential amplifier A1, a series-pass element Q1, an inverter amplifier A3, and an emitter follower Q4.

3-26. The reference amplifier A2 contains matched zener and transistor elements which produce a time and temperature stabilized reference voltage. The zener element receives a portion of its bias current from the +23.4V supply through R4 and CR1. The amplifier element receives collector current from the same source through R5. Base current for this amplifier is provided through a divider composed of R9, R14, R16, R56 and R59. This divider is connected to the $+V_{REF}$ sense line. The FET switches, Q2 and Q3, provide separate output and sense connections when a positive V_{REF} is called. Should any variations occur on the $+V_{REF}$ sense line, A2 will amplify them with respect to the zener element reference. The change is then applied to one input of A1 which also receives a sample of the $+V_{REF}$ line from the divider composed of R2 and R3. A1 in turn amplifies the change and alters the conduction of Q1 to maintain a constant +10V output for $+V_{REF}$ sense. Variable resistor R9 allows adjustment of the sense line input to A2 and subsequently the $+V_{REF}$ sense level.

3-27. The inverter amplifier composed of A3 and Q4 produces a $-V_{REF}$. A3 is connected as an inverting, unity gain, amplifier. Emitter follower Q4 functions as an output buffer. Feedback through R19 and R18 controls the overall gain of both amplifiers. Variable resistor R19 adjusts this feedback level and subsequently the resultant $-V_{REF}$ sense output level. Resistors R6 and R21 compensate for TC factors associated with FET gates in the ladder section driven by V_{REF}.

3-28. GATE DRIVERS. The Gate Drivers of Q7 through Q11 control the conduction of the FET switches associated with the V_{REF} Supply. When the power source has a positive output programmed, the command at pin 18 is low (−5V), thus turning on Q8, Q11 and switching off FET gates Q2, Q3. With Q8 on, the emitter-base junction of Q9 is reverse biased causing Q9 and Q10 to turn off, thus turning on FET gates Q5, Q6, and Q25. The V_{REF} output applied to pin D is therefore −10V when a positive output

is programmed. Should a negative output be programmed, the command at pin 18 is high (0V), which turns off Q8 and Q11 and switches the FET gates Q2 and Q3 on. With Q8 cut-off, Q9 conducts and turns on Q10, thus switching the FET gates Q5, Q6, and Q25 off. As a result, the voltage at pin D is +10V when a negative output is called. Should the STANDBY or EXT REF mode be programmed, low (−5V) commands exist at pins S or V. These low inputs will turn on Q7 and Q8, thus turning on both Q10 and Q11 and switch all FET gates off. As a result the V_{REF} supply is completely disconnected from the V_{REF} output terminals, B and D.

3-29. RELAY DRIVER. The Relay Driver composed of Q19 and Q20 is used to energize K1 when the power source is turned on. The contacts of K1 then complete the connections to the OUTPUT connector. Should the power source be shut off for any reason, the connections are broken and the load is not subjected to any unprogrammed voltage.

3-30. A4 External Reference (4210A-1041)

3-31. The A4 External Reference is installed as the −03 Option. It receives and processes an external reference input having a frequency of dc to 30 kHz and a level from 0 to ±14.5V dc or peak ac. The circuitry consists of three differential amplifiers and an emitter follower which form an operational amplifier. FET gates Q9 and Q10 controlled by drivers Q11 and Q12 apply the amplifier output and sense line to the V_{REF} line in the A3 Preamplifier.

3-32. DIFFERENTIAL AMPLIFIER. The Differential Amplifier consists of three individual amplifiers: Q1 through Q8 and the emitter follower Q13. The external reference input is applied through R1 and C9 to one input of the differential FET, Q1. This stage amplifies the input in respect to V_{REF} common and provides a differential input to Q5. Feedback through R16 and R17 maintains the input of Q1 at virtual V_{REF} common. Adjustment of R17 controls the overall gain and subsequently the output V_{REF} high at terminal 4. Variable resistor R6 allows zero offset adjustment of the output, V_{REF} high. Jumper selection of R5 and R8 through R10 provides coarse adjustment of offset. Selection of R_N and R_P in the drain circuit of Q1 is done to provide a low temperature coefficient for the offset voltage. A constant current source for Q1 is provided by Q2, while TC compensation of the current source is provided by Q3. The differential Darlington composed of Q4 and Q5 amplifies the output of Q1 and furnishes a single-ended drive signal to Q7. This drive signal is developed across Q6 which functions as a high impedance, constant current source for Q4B. The final quasi-differential amplifier Q7 and Q8 supplies a drive signal to the emitter-follower output stage of Q13. This stage provides a low impedance output to drive the V_{REF} high line. Q14 functions as a high impedance current source for Q13. Diodes CR1 and CR2 provide connection to the feedback line when Q9 and Q10 are turned off.

3-33. FET GATES. Q9 and Q10 control application of the external reference to the internal V_{REF} lines. Q9 connects the feedback line to V_{REF} SENSE, and Q10 connects the external reference to the internal V_{REF} HIGH line. Drivers Q11 and Q12 control the on/off condition of Q9 and Q10 in conjunction with the EXT REF and STANDBY commands at terminals 13 and M.

3-34. When an EXT REF command (0V) exists at terminal 13, Q11 is turned off, and $-V_A$ is applied to both the emitter and base of Q12. This condition turns off Q12 and switches FET gates Q9 and Q10 on, thus applying the external reference to the internal V_{REF} line. The same condition occurs when a STANDBY command (0V) exists at terminal M. Diodes CR3 and CR4 provide isolation between the input command lines.

3-35. Should a STANDBY or EXT REF command (−5V) exist, Q11 will be switched on and turn on Q12. Conduction of Q12 applies $-V_A$ to the gates of Q9 and Q10 which turns them off. This condition then disconnects the external reference from the internal V_{REF} lines.

3-36. A5 Binary Ladder (4216-1031)

3-37. The A5 Binary Ladder contains the lower ten segments of a 14-bit binary ladder and its associated drivers. The $V_{R'}$ Supply, which is a unity gain buffer, is also located on this assembly. It is used to prevent loading of V_{REF} by the ladder drivers. The ladder is a binary weighted voltage divider controlled by the digital program word. The resistance and the relative position of each ladder segment, with respect to the output, determines the significance of its contribution to the total output voltage.

3-38. $V_{R'}$ SUPPLY. The $V_{R'}$ Supply composed of Q1 through Q3 is a unity gain buffer amplifier. Q3 is the buffer stage for emitter follower Q2. Diode CR1 compensates for the input offset voltage at emitter-base junction of Q2. The currents through Q2 and CR1 are held constant by the current regulator Q1. This allows the $V_{R'}$ output to closely track V_{REF} over a wide voltage range.

3-39. LADDERS. The ten lower segments of the binary ladder consist of R1 through R3, and R5 through R15. Each segment of the ladder is formed essentially by a resistor whose value is inversely proportional to its binary weight. A simplified diagram of a typical binary ladder is shown in Figure 3-3.

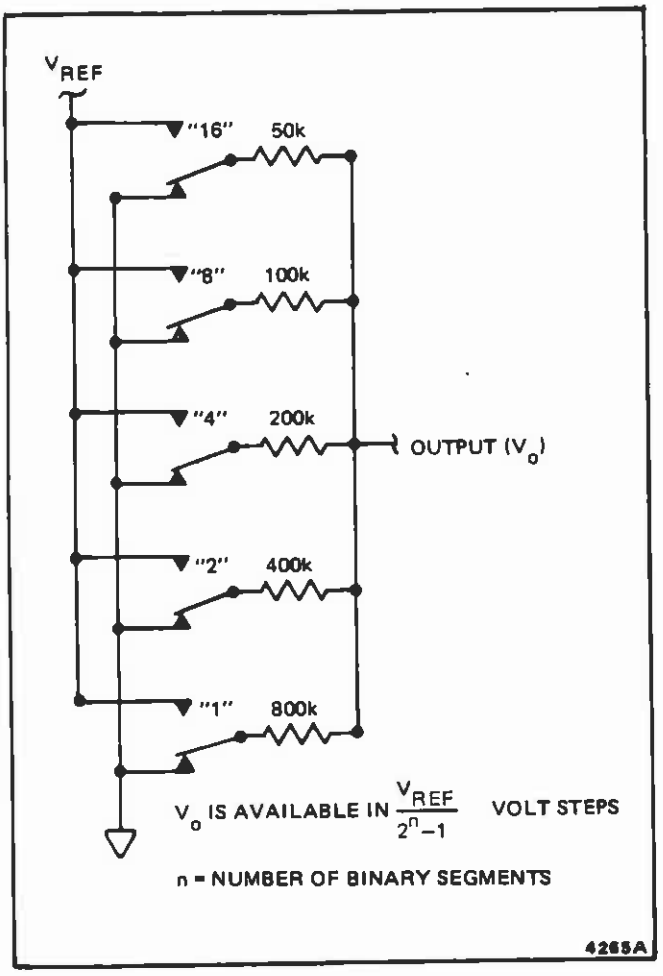


Figure 3-3. BINARY LADDER (SIMPLIFIED)

3-40. DRIVERS. Each ladder resistor is connected to V_{REF} common using a driver such as the one shown in simplified Figure 3-4. When the bit command is high (0V), QA and QC are both turned off, which applies $-V_A$ to the gate of QB and $V_{R'}$ to the gate of QD. (Since $V_{R'}$ and V_{REF} are always at the same potential the gate-to-source voltage of QD will be 0V even if an ac reference is used). This condition switches QD on and QB off, thus applying V_{REF} through QD to the ladder resistor R_N. Absence of a bit command will apply a low (−5V) to the base of QA which causes it to conduct. The resulting 0V collector signal switches on gate QB and the driver QC. Conduction

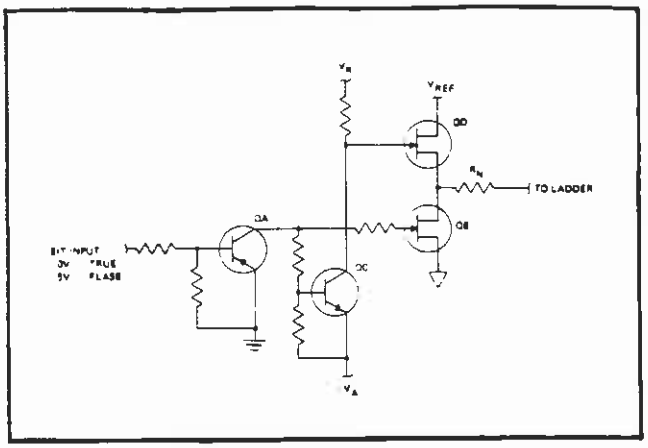


Figure 3-4. LADDER DRIVER (SIMPLIFIED)

of QC applies $-V_A$ to the gate of QD, turning it off. As a result, V_{REF} common is applied through QB to the ladder resistor R_N.

3-41. A6 Isolated Control Logic (4275A-1021)

3-42. The A6 Isolated Control Logic assembly receives and processes all input and output data at the Programming Connector, J1. A logic diagram in simplified form is shown in Figure 3-5. Logic timing is illustrated in Figure 3-6.

3-43. PRESET GENERATORS

3-44. Two Preset Generators are used in the Isolated Control Logic. Their purpose is to preset all counters, flip-flops, and registers to their proper state when the supply is first turned on. This is to insure that the output of the power source is programmed to its minimum value, and that all logic is in the proper state to accept input data and process it properly upon command. One Preset Generator is used to preset the input programming circuitry and is composed of Q8 and Q5. When input power is applied, the $+V_L$ supply rises to its regulated level of +5 volts. At this point C5 has not been charged, and Q8 and Q5 are turned off, leaving the preset line high. C5, driven by the current from the +5V supply begins to charge C5 at a linear rate. The voltage divider composed of R9 and R10 provides a +4V reference to the gate of a Programmable Unijunction Transistor, Q8. When the charge on C5 reaches approximately +4.5V, the gate of anode Q8 is forward biased causing it to turn on and latch. C5 now begins to rapidly

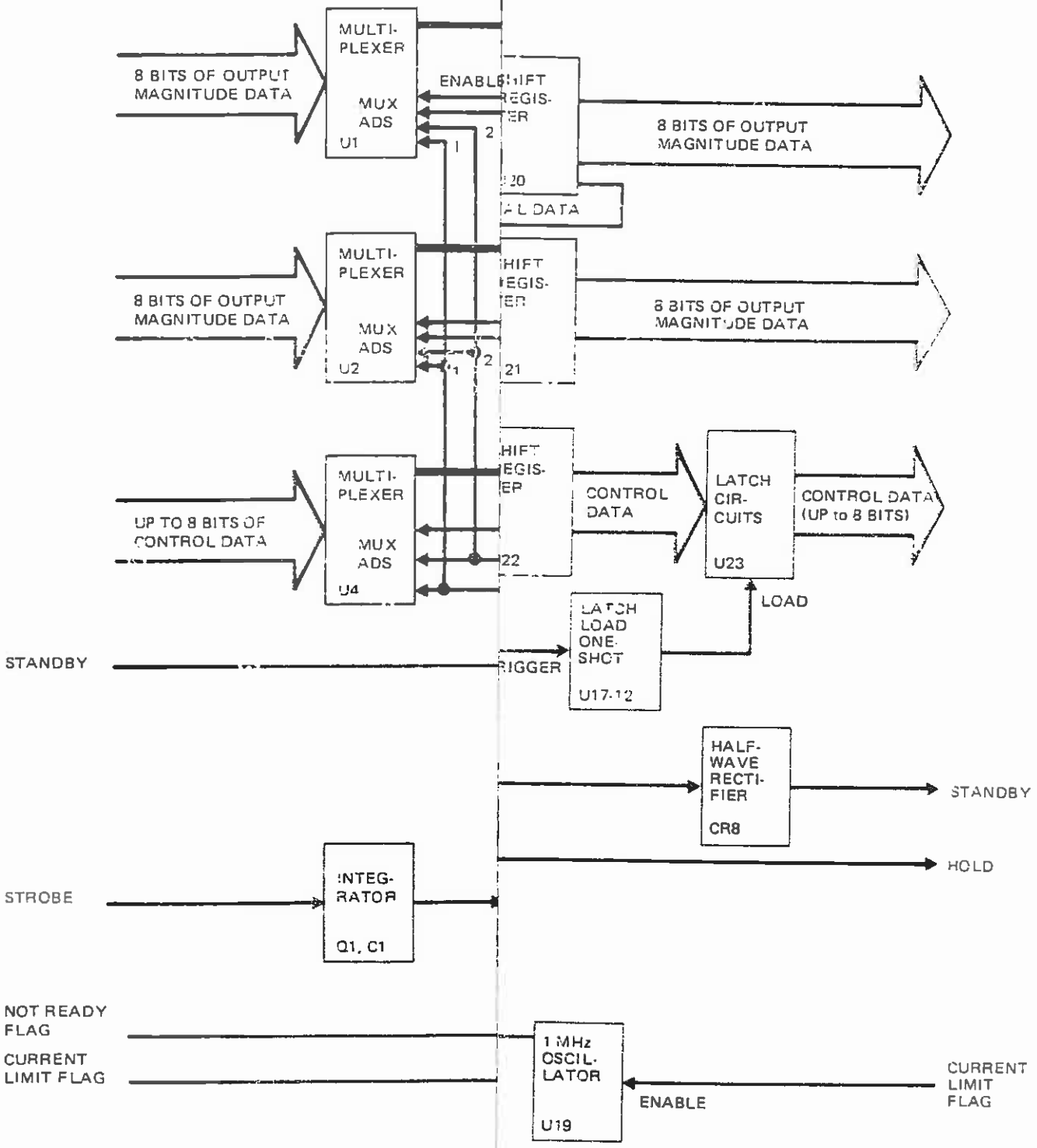


Figure 3-5. ISOLATED CONTROL LOGIC (Simplified)

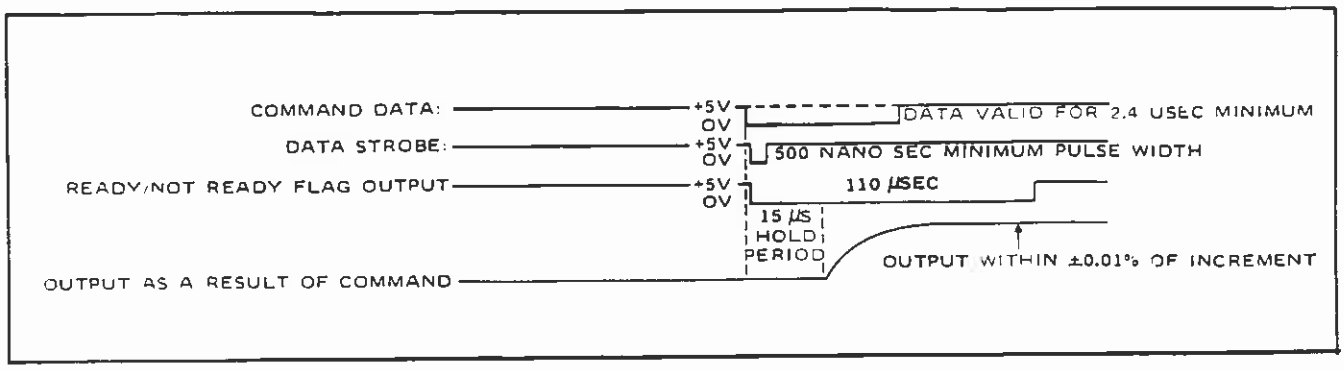


Figure 3-6. ISOLATED CONTROL LOGIC TIMING

discharge through Q8 and R11. The voltage developed across R11 is sufficient to turn on Q5, which causes the preset line to go low, thereby presetting all input programming circuitry. When the discharge of C5 is almost complete, the voltage drop across R11 can no longer supply base drive to Q5; it therefore turns off, allowing the preset line to return to its high state.

3-45. The second Preset Generator is used to preset the shift registers in the isolated portion of the logic circuitry. It is composed of Q16 and Q15 and is less complex than the preset generator previously described. When input power is applied, the $-V_L$ supply rises to its regulated level of −5V. At this time Q16 is not conducting, C33 is not charged, and the output of U15 is −1V. C33 now begins to charge at an exponential rate through R57. R54 and R55 form a voltage divider which provides a −1V reference to the gate of a Programmable Unijunction Transistor, Q16. When the charge on C33 reaches approximately −0.5V, the gate to anode of Q16 is forward biased causing it to turn on and latch. C33 now begins to rapidly discharge through Q16 and R58. The voltage developed across R58 drives the input of Q15 toward 0V, causing its output to drive close to −5V and clear shift registers U20, U21 and U22. As the discharge of C33 is almost complete, the voltage drop across R58 approaches zero volts allowing the input of Q15 to return to a −5V level. The output of Q15 then returns to 0V, completing the preset pulse. Q16, however, remains latched because of the small holding current supplied through R57.

3-46. DATA TRANSFER SEQUENCE

3-47. The parallel program data (output voltage magnitude, sign, output voltage range, current limit magnitude and external reference function) is applied to the inputs of a series of multiplexing circuits as shown in Figure 3-5. When the data is settled at the multiplexer inputs, the program source generates a strobe signal having a duration of nanoseconds or longer. The strobe pulse is fed via an integrator to the trigger input of a delay one-shot. The integrator provides noise immunity, and triggers the delay one-shot when it receives a pulse having a width of 800 nanoseconds or greater. The delay one-shot produces an 800 nanosecond pulse, the leading edge of which triggers the hold one-shot (via T5) to produce an eight or 16 microsecond pulse to the hold input of the power source. The width of the hold one-shot output pulse depends upon the particular power source model. That is, the 4210A and 4216A require an eight microsecond hold pulse, while the remaining models require a 16 microsecond hold pulse. In either case, the hold pulse is used within the A3 assembly to hold the output voltage magnitude constant while programming is underway.

3-48. The trailing edge of the delay one-shot output triggers the not ready one-shot and sets the start/flip-flop. The not ready one-shot generates a 100 microsecond pulse which becomes the not ready flag output to the program source. The not ready flag indicates that the 4200-09 is busy and not available to accept program data or strobe signals from the program source. When the strat/stop flip-flop becomes set, the Q output provides a start signal (voltage level) to the start/stop input of a 10 MHz clock. The Q output of the start/stop flip-flop is also fed to an input of gate U12-8 to gate the clock output pulses to various portions of the control logic to transfer the program data across the guard. Concurrently, the Q output of the start/stop flip-flop inhibits gate U14-3 to prevent clock pulses from reaching the primary winding of T4. (This function is described in later paragraphs.)

3-49. The 10 MHz clock pulses gated by U12-8 are fed to the input of a ÷16 (four-bit binary) counter. At the time of the sixteenth clock pulse, the counter reaches full count and generates a carry pulse to the reset input of the

start/stop flip-flop (and also to the reset input of the complement flip-flop described later). As the counter advances through its 16 states, the four binary-weighted (1, 2 4 and 8) outputs address the multiplexer channels and move the bits of data applied to the parallel inputs over to the multiplexer output. For example, the first clock pulse to the counter advances it from the zero state to the first state in which the "1" output is true and the "2", "4" and "8" outputs are false. As a result, the second channel of U1 and U4 is addressed, and the second bit of data appears at the multiplexer outputs. As the counter advances, the subsequent inputs of U1 and U4 appear at the multiplexer outputs, until the count of eight is reached. At this point, the "8" output becomes true to inhibit U1 and enable U2. The eight inputs of U2 are sequentially addressed in the same manner as U1 and the program data appears in serial format at the U2 output, and is commonly connected with the U1 output. During the 16-state cycle of the counter, U1 and U2 are each cycled once, while U4 is cycled through its eight addresses twice. This is of no consequence since input data has not changed during the generation of the 16 clock pulses.

3-50. The 16 clock pulses are fed to inputs of gates U13-3 and U13-5 to gate the serial program data appearing at the multiplexer outputs to the primaries of T1 and T3. The clock pulses are also fed directly to the primary of T2. The transformers couple the signals across the guard. On the inside of the guard, the clock pulses are applied to three eight-bit shift registers causing the registers to load the serial program data. Shift registers U20 load the 16 bits of output magnitude data while U22 loads (twice) up to eight bits of control data. The parallel outputs of U20 and U21 are applied directly to the ladder network assembly (A5), while the parallel outputs of U22 are applied to a series of latch circuits. To load the control data into the latch circuits, the first of the 16 clock pulses triggers a latch-timing one-shot which has a period of two microseconds. This one-shot is not re-triggerable by the subsequent clock pulses, and the trailing edge of the output pulse occurs after the clock pulses and serial transfer of data into the shift registers is complete. The trailing edge triggers the latch load one-shot to parallel load the eight bits of control data from the shift register into the latch circuits for application to the control circuits within the power source.

NOTE!

Complementing magnitude data occurs only in binary-type power sources.

3-51. COMPLEMENTING BINARY DATA

3-52. Binary-type power sources require that negative values of magnitude data be two's complemented since binary program sources usually indicate polarity by means of a single bit and supply two's complemented magnitude data for negative outputs. The binary-type power sources require non-complemented binary data plus a polarity bit. As a result, negative binary magnitude data, consisting of complemented data, must be re-complemented to satisfy the requirements of the power source. When the binary program source indicates negative sign, gate U9-8 is enabled to pass the output of the complementing logic. The complementing logic receives the serial output of U1 and U2, complements it, and passes it across the guard via T1.

3-53. Operation of the two's complementing logic (U9 and U10) is such that the first bit of serial data (multiplex address zero) is present at the output of multiplexer, U1, before the ÷16 counter and a complement flip-flop (U10) receives the first of 16 clock pulses. At this time, the ÷16 counter is in its zero state to address channel zero of U1, and the complementing flip-flop is still reset (as a result of the carry pulse generated by the ÷16 counter at the end of the previous data transfer sequence). With the complement flip-flop reset, the complement logic is not enabled and no inversion of serial data takes place. This condition permits the first binary magnitude data to be transferred without being complemented. However, after the first clock pulse, the complement flip-flop may be allowed to go set (to enable the complement logic) depending upon the state of the J input, which is derived from the serial data. As a result, the complement flip-flop goes set at the time of the first true bit of serial data is enable the inverting logic and complement the remaining bits of serial data. After the 16th bit of data, the complementing flip-flop is reset by the carry output of the ÷16 counter.

3-54. STANDBY OPERATION

3-55. The power source can be commanded to standby or operate mode at anytime by the program source. As shown in Figure 3-5, the standby command (dc) is gated to the start input of the 10 MHz clock. The clock is turned on and generates pulses as long as the standby signal is present. The start/stop flip-flop remains reset from the last transfer sequence to enable gate U14-3 and pass the clock pulses via T4 to a half-wave rectifier on the inside of the guard. The dc output of the rectifier becomes the standby signal for control of the power source. During standby operation, data transfer does not take place due to the

start/stop flip-flop being reset and gate U12-8 being inhibited.

3-56. CURRENT LIMIT FLAG

3-57. The current limit flag produced by the A9 Power Amplifier whenever the power source is in the current limit mode, is used to enable a 1MHz oscillator (U19) which produces pulses at a 1MHz rate. The pulses are fed via T6 to the trigger input of a re-triggerable one-shot having a period of 1.1 microseconds. As long as the 1MHz pulses occur, the output of the re-triggerable one-shot is held at dc level which becomes the current limit flag to the program source.

3-58. A3 Preamplifier (4265A-1051)

3-59. The A3 Preamplifier produces a drive signal proportional to the input programming commands. This drive signal is applied to the A9 Power Amplifier which, in turn, produces the power source output. The circuitry consists of the four most significant bits of the binary ladder and associated switches and drivers, ladder clamps, voltage range switches, high impedance input stage, sample and hold, and output stage.

3-60. BINARY LADDER. The four most significant bits of the Binary Ladder consist essentially of R26, R27, R29, and R31. Their individual resistance values weigh the division factor necessary to scale V_{REF} in respective 8192, 4096, 2048, and 1024 portions. Selection of individual ladder resistors is done through associated ladder switches. Variable resistors R28, R30, and R32 allow precise calibration of the 4096, 2048, and 1024 ladder portions to the 8192 portion. The resulting scaled V_{REF} from these ladder portions is combined with the A5 Binary Ladder input through R25 and applied to the input of Q18A. Feedback from the HIGH SENSE terminal at the output of the power source through resistances selected by the Voltage Range Switches drives the input to Q18 to virtual analog common, in the manner of a high-gain operational amplifier.

3-61. LADDER SWITCHES and DRIVERS. The Ladder Switches and Drivers Q1 through Q16, apply V_{REF} or analog common V_A common, to the ladder resistors under control of the 8192, 4096, 2048, and 1024 bit commands. Each Ladder Switch-Driver combination functions in the same manner; thus only operation of the 8192 bit is described.

3-62. The 8192 ladder resistor is connected to V_{REF} or analog common through Q1 and Q2 or Q3, respectively. When an 8192 command (0V) exists at terminal 18 of P1, both Q4 and Q5 will be switched off. Q3 is switched off by its resulting $-V_A$ gate voltage and Q1, Q2 are switched on by the resulting $V_{R'}$ gate voltage. With Q1 and Q2 conducting, V_{REF} is applied to R26. Absence of an 8192 command applies −5V to terminal 18 of P1 and switches Q4 and Q5 on. The resulting 0V gate voltage at Q3 switches it on and applies analog common to R26. Q1 and Q2 are switched off by conduction of Q5, which applies $-V_A$ to their gates.

3-63. LADDER CLAMPS. The Ladder Clamps consisting of CR5, CR6, R47 and R48 limit the summing junction voltage at the input of Q18. Clamp signals at terminals 7, 19, and W of P1 turn on CR5 or CR6 during a current limit condition. This minimizes any output voltage transients at the output of A9 Power Amplifier if the load causing the current-limit condition is suddenly removed.

3-64. VOLTAGE RANGE SWITCHES. The Voltage Range Switches and Drivers consisting of Q30 through Q34 select the appropriate feedback resistance and frequency compensation for the 16V and 65V range. In the 16V range, a −5V command is present at terminal 14 and R of P1. This voltage turns off Q34 and Q33, which, in turn, switch on FET gates Q30 through Q32. Conduction of Q31 and Q32 connects R39, R40, R42, and R43 across R36 and R35. The end of this network that connects to pin 4 of P1 ultimately becomes the HIGH SENSE terminal at the output of the power source. The frequency response of the Preamplifier in both voltage ranges is controlled by Q30. In the 16V range, conduction of Q30 by-passes R34 and C2, thus connecting only R33 and C1 to the Preamplifier output. In the 65V range, a 0V command at terminal 14 and R of P1 turns on Q34 and Q33 which turns off Q30 through Q32. With Q31 and Q32 off, only R35 and R36 are connected to the power source output (HIGH SENSE), thus increasing the total feedback resistance by four. The resulting output voltage is subsequently four times the binary input commands. With Q30 off in the 65V range, R33, C1 and R34, C2 are connected in series to establish the desired frequency response.

3-65. HIGH IMPEDANCE INPUT STAGE. Differential amplifier Q18 amplifies the Binary Ladder output with respect to analog common, V_A common, such that feedback through resistance selected by the Voltage Range Switches produces a virtual analog common at the input of Q18A. Transistor Q19 functions as a constant current source, and

Q20 provides temperature compensation. Variable resistor R61 provides adjustment to compensate for the input offset of Q18. Jumper selection of R57 through R59 and R62 provides coarse offset adjustment. Selection of R_P and R_N in the drain circuit of Q18 is done to provide a low temperature coefficient of input offset voltage. Diodes CR7 through CR12 limit the maximum voltage swing applied to the following stage.

3-66. SAMPLE AND HOLD. The Sample and Hold circuitry consists of MOSFET gates Q21, Q22, driver Q23, and capacitors C1 and C11. These capacitors provide memory during programming changes. Normally, a HOLD command (0V) is present at terminal P of P1 and Q23 is conducting. This condition turns on Q21 and Q22 and the output of Q18 is amplified by Q24, Q25. During programming changes, however, presence of a HOLD command (−5V) at terminal P of P1 turns off Q23 and Q21, Q22. Capacitors C1 and C11, which are connected to the inputs of Q24, then hold a sample of the last input from Q18 and hold the output voltage relatively constant for the duration of the HOLD command. The HOLD period is short enough and the circuit constants are chosen so that negligible output voltage change occurs. A secondary HOLD circuit composed of U1 and Q35 through Q37 provides a clamp to analog ground at the input of Q18 during the HOLD period. Presence of a HOLD command (−5V) presets J-K flip-flop U1 to provide a low Q output, which turns on Q37. Q36 is switched on by the resulting $-V_L$ common base signal and turns on Q35, which applies analog common to the base of Q18.

3-67. Transistor Q26 functions as high impedance constant current source for Q25B. Q27 and Q28 amplify the output of Q25B and furnish a drive signal to Q29.

3-68. OUTPUT STAGE. Emitter follower Q29 provides a low impedance output signal at terminal 5 of P1. This signal is applied to the A9 Power Amplifier which then produces the power source output.

3-69. A9 Power Amplifier (4265A-1071)

3-70. The A9 Power Amplifier produces the final output voltage and current of the power source. It also provides both source and sink current limit protection of the bipolar output. The circuitry consists of an input amplifier, driver, clamp circuitry, current sources, output stage, and current limit detector.

3-71. INPUT AMPLIFIER. The Input Amplifier composed of Q9 through Q11 and Q20 through Q25 amplifies the input appearing at terminal D of P1. The resulting voltage at the emitter of Q11 corresponds closely to the programmed output voltage. A closed-loop dc gain of five is established by feedback through R62 and R21. Overall frequency response is controlled to 6 db per octave by C6. Amplifiers Q22 and Q23 link V_U common to the A3 Preamplifier common (V_{REF} common) such that current flow between these two points is minimized. Q20 and Q21 provide current with respect to the common established by Q23, Q22 emitters. Emitter follower Q9 and amplifier Q10 provide voltage gain and a drive signal to the output emitter follower Q11. Overall frequency response to this point is controlled with feedback through C6. The resulting emitter voltage of Q11 is close to the final output voltage of the power source. Transistors Q24 and Q25 function as current sources for Q10 and Q11, respectively.

3-72. DRIVER. The Driver consisting of Q12 and Q26, form complementary current amplifiers. These amplifiers receive a bipolar drive voltage from Q11 and together with the CURRENT SOURCES produce respective drive currents for the output stage. The voltage drops across Q13, CR33, Q17, and CR27 together with variable resistor R51 set the bias current required for the output transistors Q32, Q33, Q41, and Q42. Q13 collector current is turned off when a (+) current limit condition exists and Q17 is affected similarly for a (−) current limit. These collectors drive the CURRENT LIMIT DETECTOR.

3-73. CLAMP CIRCUITRY. Voltage transients that would occur during a current limit and abrupt load removal are limited by the Clamp Circuitry. Two circuits titled + Clamp and − Clamp limit the bipolar transients. The + Clamp consists of Q1 through Q4. Transistors Q5 through Q8 form the − Clamp. Since operation of each circuit is the same, except for polarity, only the + Clamp is described.

3-74. The +Clamp monitors the voltage between the emitter of Q11 and that on the anode of CR33. Normally, Q1 and Q2 are cut-off and Q3 is conducting; however, when a current limit occurs, the anode voltage of CR33 decreases through action of either the built-in current limiter (overload protection) or the A8 Programmable Current Limiter (optional) and subsequently turns off Q3. The voltage at the emitter of Q11, will increase toward $+V_U$ during current limiting and this turns on Q2. Conduction of Q2 turns on Q1 and produces a clamp signal at terminal 6 of P1. This clamp signal then limits the summing junction voltage in the A3 Preamplifier and causes the emitter voltage of Q11 to be clamped to a voltage slightly above that of the base drive to the Output Stage. Transistor Q4 functions as a current source for Q2 and Q3. Frequency and phase

characteristics of the + Clamp circuitry is determined by C1, C2, C26 and R65.

3-75. CURRENT SOURCES. Constant current for the Output Stage is provided by the Positive and Negative Constant Current Sources. Transistors Q27 through Q30 form the Positive Constant Current Source. The Negative Constant Current Source Consists of Q36, Q38, Q39, and Q40. Since operation of each circuit is the same, except for polarity, only the Positive Constant Current Source is described.

3-76. The Positive Constant Current Source produces a constant reference current for the base of Q31. Zener CR23 produces a fixed bias for Q29, which provides a constant current through CR21, CR22, Q27, and R32 regardless of variations in $\pm V_U$. Subsequently, Q28 and Q30 receive fixed base current through these elements. The resulting constant current through Q28 and Q30 then provides a constant reference current for the base of Q31. Temperature compensation of the V_{BE} of Q28 is provided by diode-connected Q27.

3-77. OUTPUT STAGE. The Output Stage consisting of Q31 through Q35 and Q37 through Q42 produces the power source output. It also provides both sourcing and sinking current limit protection.

3-78. Transistors Q31 through Q33 and Q37, Q41, Q42 form a complementary, emitter follower stage. Q31 through Q33 produce the positive output and Q37, Q41, Q42 the negative. Total output current flows through R43, R44 (positive) and R47, R48 (negative).

3-79. Both sourcing and sinking current limit protection is provided for each section of the output amplifier. Q34 protects the positive output section and Q35 the negative. Maximum output current (sourcing) is limited to 1.2A. Sinking current is limited at a lesser value depending on the programmed output voltage. Since operation of each current limiter is the same, only the positive output section protected by Q34 is described.

3-80. Output current passes through R43 and R44. This current produces a bias voltage for Q34. When the output current (sourcing) exceeds 1.2A, the resulting potential turns on Q34. Conduction of Q34 via CR34 shunts any further base drive current to Q31, thus limiting the maximum sourcing output current at 1.2A. In the sinking mode, output current will pass through R43 and R44 to the output as above, but the output voltage polarity is zero or negative by definition. Under this condition, negative voltage more than −0.6V at the output will turn on CR25 which supplies base current for Q34 through R41 from common and adds to that supplied from the voltage drop across R4 and R44. Therefore, the base current is dependent on both sinking voltage magnitude and output current. Current limiting in milliamperes is equal to $1000\text{-}10E_{out}$.

3-81. When the A8 Programmable Current Limiter −06 Option is installed, ±I LIMIT inputs are applied to terminals 2 and 10 of P1. These inputs clamp the maximum base drive to both sections of the Output Stage in a similar manner to Q34, thus limiting the maximum output current at a level determined by the input current limit commands.

3-82. CURRENT LIMIT DETECTOR' The Current Limit Detector produces an I LIMIT (0V) command at terminal 14 of P1 whenever a source or sink limit condition exists. Circuitry consists of Q14 through Q16, Q18, and Q19. Positive output section limiting is detected by Q14. Limiting in the negative output section is detected by Q18. Transistors Q15, Q16, and Q19 are drivers.

3-83. Under normal operating conditions Q14 and Q18 are turned on by conduction of Q13 and Q17 in the Driver. Transistors Q15 and Q19 are switched off by conduction of Q14 and Q18, thus turning Q16 on and producing an I LIMIT (−5V) command at terminal 14 of P1. Should a current limit occur in the positive or negative section of the Output Stage, the associated Q13 or Q17 in the Driver will be turned off. This turns off Q14, Q15 or Q18, Q19, thus turning Q16 off and producing an I LIMIT (0V) command at terminal 14 of P1.

3-84. A8 Programmable Current Limiter (4250A-1081)

3-85. The A8 Programmable Current Limiter is installed as the −06 Option. It compares the voltage from a ladder network to an input voltage proportional to the output current. When the output current exceeds the ladder network reference, a clamp signal is produced that is used to limit the output current of the A9 Power Amplifier. The A8 Programmable Current Limiter contains the following circuitry: an 8-4-2-1 to 4-4-2-1 binary code converter, FET drivers, a ladder voltage reference, ladder switches and a ladder, a programmable reference and programmable reference inverter, and two current limit comparators - one positive and the other negative. Auxiliary circuits are a ground isolator and two power supplies, one 15 volts and the other −16 volts. A one-ohm current sampling resistor is tied to the input of the two current limit comparators.

3-86. 8-4-2-1 to 4-4-2-1 CONVERTER. This logic converter consists of two, digital integrated circuit, hex-inverters U1A through U1F and U2A through U2F. They convert the input 8-4-2-1 code to 4-4-2-1 code, and in the absence of any programmed inputs, program the ladder to the lowest current limit, 10 milliamps. This is the quiescent state of the limiter in which ladder switch Q4 and the current range switch Q26 are turned on, placing operational amplifier U4 in low range. This ensures that the Model 4265A current limits at the lowest current, 10 milliamps, as a safety feature. In the event a programmed input for 80 milliamps is applied to the converter, the logic input is applied to two circuits, one directly to the base of FET Driver Q13 and the other indirectly through two inverters U2F and U1A to the base of FET Driver Q10. These two drivers turn on ladder switches Q9 and Q12 and two code 4 ladder resistors, thereby applying an equivalent 8 to the Programmable Reference amplifier and establishing a current limit of 80 milliamps.

3-87. FET DRIVERS. The ladder FET DRIVERS consist of PNP-NPN Transistor pairs Q3-Q5, Q7-Q8, Q13-Q14, and Q10-Q11. The emitters of these pairs as well as the current range FET drivers Q15-Q16, are returned to V_L common through a ground isolator network consisting of transistors Q1 and Q2. The ground isolator network is described later. The purpose of the drivers is to increase the voltage output of the converters to a level required by the FET switches.

3-88. LADDER VOLTAGE REFERENCE. The Ladder Voltage Reference consists of a temperature compensated, 6.3 volt zener diode CR7 and produces a stable reference voltage that is reduced to 0.1 volt at TP3 by resistors R4, R6, and R59. This voltage reference is supplied by the regulated +15 volts power supply (TP2) consisting of 16 volt zener CR1, transistor Q28, and associated components.

3-89. LADDER SWITCHES AND LADDER. The Ladder Switches and Ladder, respectively, consist of FET switches Q4, Q6, Q12, and Q9 and resistors R52, R55, R54, and R15. The ladder resistors are weighted in a ratio of 1, 2, 4, and 4. The ladder operation is best explained in conjunction with the Programmable Reference. (See paragraph 3-96).

3-90. PROGRAMMABLE REFERENCE AMPLIFIER. Programmable Reference Amplifier U4 is a monolithic IC operational amplifier. Assuming current range switch Q26 is on, then U4 output voltage varies between −0.01 volt and −0.11 volt as the ladder resistors are switched into the circuit by the FET switches. That is, with only Q4 on, the output voltage is −0.01 volt. With Q4, Q6, Q12, and Q9 on, the output voltage is −0.11 volt. The range is set by R31 in parallel with R30 and is the 10 ma to 110 ma current range. With Q26 turned off, the range is determined by R30 alone. This is the 100 ma to 1.1 ampere range (Current Limit x 10 command) in which the ladder resistors produce an output from U4 of −0.1 volt to 1.0 volt. Amplifier U3, also a monolithic integrated circuit, together with resistors R24 and R25, forms a unity gain, inverting amplifier. The output of U3 is the same magnitude as that of U4, but of opposite polarity.

3-91. POSITIVE AND NEGATIVE I LIMIT COMPARATORS. Since the comparators function in the same manner, except for polarities, only the positive comparator is described. The output current from the Model 4265A flows through a one-ohm resistor, R51. A *positive* output current through this resistor produces a positive voltage that is compared to the output of U3 by action of transistor Q17. When the positive output of U3 is greater than the positive voltage developed across R51, Q17B is on and Q17A is off, as are Q18, Q19, and Q17. This corresponds to the Model 4265A output current being less than the programmed I-limit. When the positive output of U3 is less than the positive voltage developed across R51, Q17A, Q18, Q19, and Q27 are all on and conducting. The greater the difference between the R51 and U3 voltages, the greater these transistors conduct. The collector of Q27 connects, by way of pin 2 of P1, to the base of Q31 on the A9 Power Amplifier. When the Q27 collector conducts, it shunts base current drive away from Q31, as described in paragraph 3-87, thus limiting the Model 4265A output current to the programmed level. Transistors Q18 and Q27 are common-base stages used as voltage translators: Q18 from the −10 volts level of Q17A to Q19 which is referred to V_U (about −100 volts), and Q27 from Q19 to essentially the OUTPUT HIGH terminal voltage. Transistor Q19 provides current gain and Q20 is used as a temperature compensating diode for Q19. Capacitor C4 and resistor R40 are the primary frequency response determining components. Transistor Q25A and Q25B compares a negative reference voltage to negative voltages produced across resistor R51 by the output current in a manner similar to Q17A and Q17B. Transistors Q24, Q21, Q23, and Q22 correspond in function to Q18 through Q20 and Q27, respectively.

3-92. GROUND ISOLATOR. The Ground Isolator circuit, composed of transistors Q1 and Q2 isolate the ground currents flowing in V_U COMMON from those in V_L COMMON. The input logic lines driving the first transistor of each pair of FET Drivers (the emitters of the drivers) are referenced to V_L COMMON indirectly through transistors Q1 and Q2. Thus, the only current through the point of commonality of V_L - V_A - V_U is the base

current of Q1 and this has but a negligible effect in the OUTPUT LOW sense line.

3-93. MINUS 16 VOLTS POWER SUPPLY. Diode CR2, a 16 volt zener, produces −16 volts at test point 4. This voltage is used in the Ground Isolator, the FET Drivers, and U3 and U4.

Section 4
Maintenance

4-1. INTRODUCTION

4-2. This section contains servicing information for the Model 4265A. Table 4-1 lists the required test equipment. If the recommended equipment is not available, substitute equipment with equivalent specifications can be used.

Table 4.1 RECOMMENDED TEST EQUIPMENT

NOMENCLATURE	EQUIPMENT
AC/DC Voltmeter	FLUKE Model 887A
Manual Control Unit (MCU)	FLUKE Model A4200
*AC Source, 100 Hz, 30 kHz	FLUKE Model 510A (2)
**Resistive Load	10 ohm ±1%, 20w

*Required only if –03 Option is installed.
**Required only if –06 Option is installed.

4-3. SERVICE INFORMATION

4-4. All products manufactured by the John Fluke Mfg. Co., Inc. are warranted for a period of one year. Complete warranty information is located in the WARRANTY at the front of the manual.

4-5. Factory authorized calibration and service is available at various world-wide locations. A complete list of Factory Authorized Service Centers is located at the rear of the manual. If requested, an estimate will be provided before repair work is done on an instrument that is beyond the warranty period.

4-6. GENERAL MAINTENANCE

4-7. Cleaning

4-8. This power source should be cleaned periodically to remove dust, grease, or other contaminates. The exterior can be cleaned with a cloth moistened with anhydrous ethyl alcohol or Freon T.F. Degreaser (MS 180) Miller Stephensen Chemical Co., Inc.) If either of these cleaning agents are not readily available, soap and water applied sparing to a cloth can be used. Cleaning of the interior sections is done using clean, dry air at low pressure.

4-9. Air Filter Cleaning

4-10. An air filter is installed on the rear panel blower assembly. This air filter should be removed and cleaned periodically to remove accumulation of dust and grease. The air filter is easily removed by pulling it free from the blower assembly. Cleaning is done using solvent and a brush or mild soap and warm water.

4-11. Fuse Replacement

4-12. The input power fuse is located on the rear section of the power source. If replacement is necessary, use the following rated fuse:

115V AC LINE	230V AC LINE
2A, AGC	1A, AGC

4-13. MAINTENANCE ACCESS

4-14. Access to the interior section of the power source shown in Figure 4-1 is done as follows:

a. Disconnect the power cord from line power.

b. Remove the top dust cover. Access is now provided to calibration adjustments and test points. Adjustments are labeled on the two inner covers.

c. Remove the two inner covers. Access is now provided for removal of the A3 through A5 or A8 pcb assemblies.

d. Removal of an A3 through A5 or A8 pcb assembly is done using a gentle rocking motion and even pulling force.

NOTE!

PCB assemblies can be mounted on an Accessory Extender card for servicing. Information regarding the Extender card is given in Section 6.

e. Removal of the A9 pcb assembly is done by first removing the screws which attach the heat sink to the bottom inner chassis. The pcb is then removed in the same manner as described in step d.

f. Removal of the A2 or A6 assembly is done from the rear panel. First remove the mounting screws at the rear panel and then pull the pcb assembly out through the rear panel.

NOTE!

The A2 pcb must be mated with the A10 pcb for servicing. An interface cable is available from the John Fluke Mfg. Co., Inc.

g. Access to the A1 and A7 pcb assemblies is possible after removing the front panel. First, remove the bottom dust cover and then remove the rack ears, if installed, from the front corner side panels. If the rack ears are not installed, peel the decals from the front corner panels. Next, remove the mounting screws which hold the transformer bracket to the A1 pcb assembly and then remove the screws from the front corner side panels. Pull the entire front panel assembly free of the instrument. Separation of the A1 and A7 pcb assemblies from the front panel is done by removing the large screws located on the A1 pcb. The A1 and A7 pcb assemblies can then be separated by removing the small screws on the A1 pcb and then pulling the pcb assemblies apart.

NOTE!

A grounding jumper located adjacent to the A2 pcb and transformer plugs into the A1 pcb. Ensure that this jumper is connected during installation.

h. Removal of the air filter and blower is done from the rear panel. First remove the air filter which snaps in place on the blower assembly. Next, remove the mounting screws which attach the blower cover to the rear panel and then remove the cover. Remove the screws which attach the blower to the rear panel and remove the blower. The interconnecting wiring is of sufficient length to allow servicing of the blower without disconnection.

4-15. CALIBRATION PROCEDURES

4-16. The power source should be calibrated every 90 days or annually, as desired, or whenever repairs have been made. Recommended test equipment is listed in Table 4-1. If the recommended test equipment is not available, substitute equipment having equivalent specifications can be used. Assembly, adjustment, and test point locations are shown in Figure 4-1. Binary and two's complement coding is shown in Table 4-2. This table provides a convenient reference for deriving two's complement coding required for negative outputs when the Isolated Logic (–01 Option) is installed.

4-17. Initial Procedure

a. Turn off the power source and then remove the top dust cover screws. Leave the cover in place.

b. Connect the Model A4200 (MCU) to the PROGRAMMING CONNECTOR on the rear panel of the power source.

CAUTION!

Ensure that the ±OUTPUT and SENSE terminals are properly connected on the rear panel of the power source.

c. Turn on the power source and select the Manual Mode and +0V output on the MCU.

NOTE!

Refer to A4200 subsection in Section 6 for operating instructions regarding MCU.

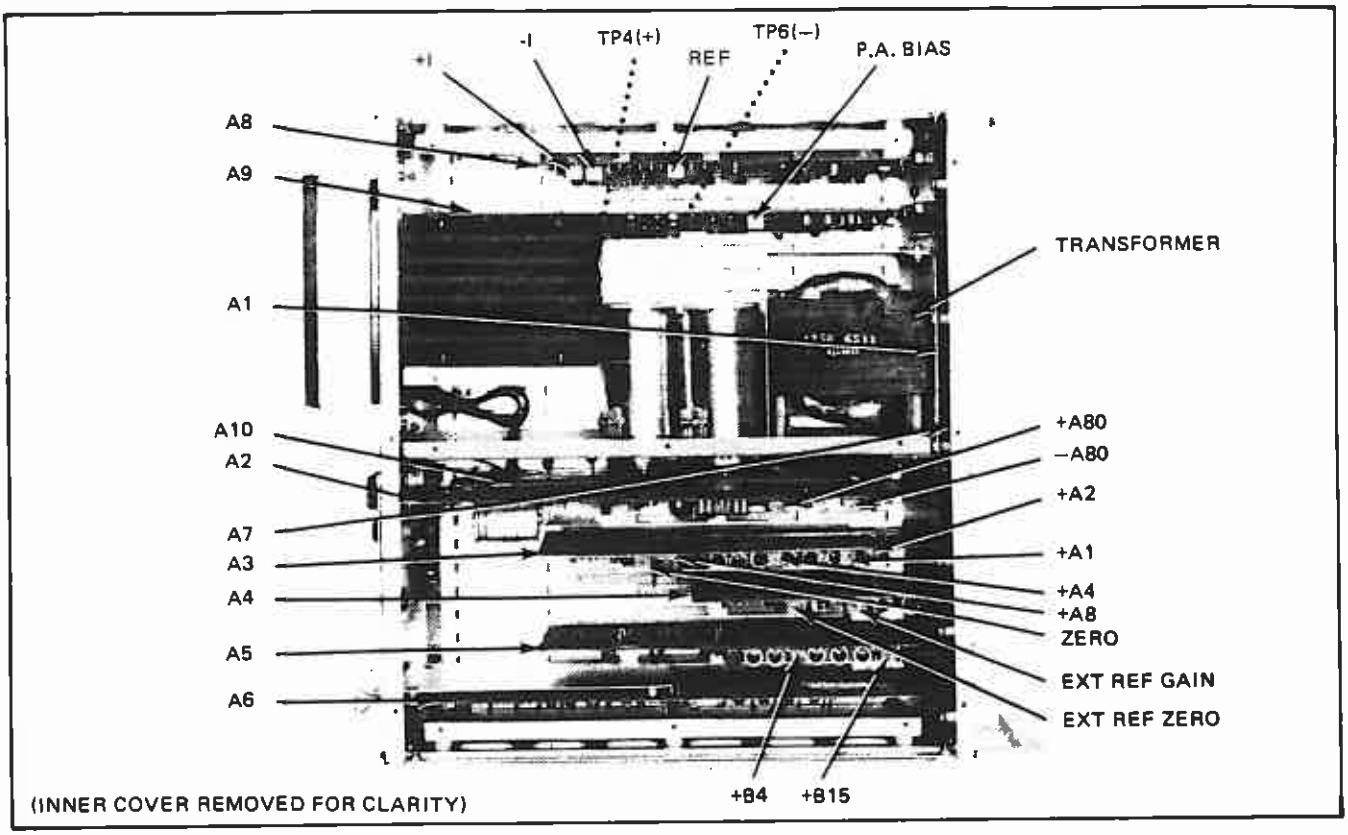


Figure 4-1. ASSEMBLY, ADJUSTMENT, AND TEST POINT LOCATIONS

TABLE 4-2. BINARY AND TWO'S COMPLEMENT CODING

BINARY CODE	OUTPUT VOLTAGE (VDC)		TWO'S COMPLEMENT CODE (NEGATIVE OUTPUT)
	16V RANGE	32V RANGE	
S B 4 2 1 I 1 0 0 0 5 2 1 G 8 4 2 1 6 2 8 3 1 N 2 8 4 2 6 4 2 8 4 2 1			S B 4 2 1 I 1 0 0 0 5 2 1 G 8 4 2 1 6 2 8 3 1 N 2 8 4 2 6 4 2 8 4 2 1
0 0 0 0 0 0 0 0 0 0 0 0 0 0 1	0.001	0.004	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
0 0 0 0 0 0 0 0 0 0 0 0 0 1 0	0.002	0.008	1 1 1 1 1 1 1 1 1 1 1 1 1 1 0
0 0 0 0 0 0 0 0 0 0 0 0 1 0 0	0.004	0.016	1 1 1 1 1 1 1 1 1 1 1 1 1 0 0
0 0 0 0 0 0 0 0 0 0 0 1 0 0 0	0.008	0.032	1 1 1 1 1 1 1 1 1 1 1 1 0 0 0
0 0 0 0 0 0 0 0 0 0 1 0 0 0 0	0.016	0.064	1 1 1 1 1 1 1 1 1 1 1 0 0 0 0
0 0 0 0 0 0 0 0 0 1 0 0 0 0 0	0.032	0.128	1 1 1 1 1 1 1 1 1 1 0 0 0 0 0
0 0 0 0 0 0 0 0 1 0 0 0 0 0 0	0.064	0.256	1 1 1 1 1 1 1 1 1 0 0 0 0 0 0
0 0 0 0 0 0 0 1 0 0 0 0 0 0 0	0.128	0.512	1 1 1 1 1 1 1 1 0 0 0 0 0 0 0
0 0 0 0 0 0 1 0 0 0 0 0 0 0 0	0.256	1.024	1 1 1 1 1 1 1 0 0 0 0 0 0 0 0
0 0 0 0 0 1 0 0 0 0 0 0 0 0 0	0.512	2.048	1 1 1 1 1 1 0 0 0 0 0 0 0 0 0
0 0 0 0 1 0 0 0 0 0 0 0 0 0 0	1.024	4.096	1 1 1 1 1 0 0 0 0 0 0 0 0 0 0
0 0 0 1 0 0 0 0 0 0 0 0 0 0 0	2.048	8.192	1 1 1 1 0 0 0 0 0 0 0 0 0 0 0
0 0 1 0 0 0 0 0 0 0 0 0 0 0 0	4.096	16.384	1 1 1 0 0 0 0 0 0 0 0 0 0 0 0
0 1 0 0 0 0 0 0 0 0 0 0 0 0 0	8.192	32.768	1 1 0 0 0 0 0 0 0 0 0 0 0 0 0

Binary Code Addition

Desired Output = 12.288V
12.288V = 8192 + 4096 bits

or

```
  0 1 0 0 0 0 0 0 0 0 0 0 0 0 0
+ 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0
-------------------------------
  0 1 1 0 0 0 0 0 0 0 0 0 0 0 0
```

Two's Complement Code Addition

Desired Output = −12.288V
−12.288V = (−8192) + (−4096) bits

```
  1 1 0 0 0 0 0 0 0 0 0 0 0 0 0
+ 1 1 1 0 0 0 0 0 0 0 0 0 0 0 0
-------------------------------
(disregard carry 1) ← 1 1 0 1 0 0 0 0 0 0 0 0 0 0 0
```

SIMPLIFIED METHOD (−12.288V)

1. Note positive output code:
   0 1 1 0 0 0 0 0 0 0 0 0 0 0 0
2. Starting from the right, copy first bit
   01(1)0000000000000 and then invert all
   remaining bits (10)1000000000000
3. −12.288V = 1010000000000000

d. Allow the power source to operate for ½ hour and then remove the top dust cover.

4-18. Power Amplifier Bias Adjustment

a. Call 65V range and a +0V output on the MCU.

NOTE!

If the A8 Current Limiter (−06 Option) is installed, call a current limit of 1.1A.

b. Connect the input of a dc voltmeter to TP4 (+) and TP6 (−) of the A9 assembly. These test points are accessible through slots in the inner cover.

CAUTION!

The test leads of the voltmeter must be fully insulated to avoid contact with the inner cover.

c. The voltage at TP4 should be +80 mV dc ±16 mV. If necessary, adjust P.A. BIAS to obtain the correct voltage.

d. Disconnect the dc voltmeter from the A9 assembly.

4-19. Zero, Reference and Bit Adjustments

a. Call 65V range and a +0V output. Also connect a dc voltmeter, observing proper polarity, to the OUTPUT terminals of the power source.

b. Adjust A3, ZERO for a 0 ±30 uV output from the power source.

c. Call 16V range and a +0V output. The output of the power source should be 0 ±10 uV. If necessary, adjust A3, ZERO until the specified outputs of step a. and c. are obtained.

d. Call 65V range and a −32.768V output (8192 bit and −SIGN bit).

e. Adjust A2, −A80 for a −32.768V dc ±1 mV output.

f. Call 65V range and a +32.768V output (8192 bit).

g. Adjust A2, +A80 for a +32.768V dc ±1 mV output.

h. Call 65V range and a +16.384V output (4096 bit).

i. Adjust A3, +A4 for a +16.384V dc ±1 mV output.

j. Call 65V range and a +8.192V output (2048 bit).

k. Adjust A3, +A2 for a +8.192V dc ±100 uV output.

l. Call 65V range and a +4.096V output (1024 bit).

m. Adjust A3, +A1 for a +4.096V dc ±100 uV output.

n. Call 16V range and a +8.192V output (8192 bit).

o. Adjust A3, +A8 for a +8.192V dc ±100 uV output.

p. Call 16V range and a +960 mV output (512, 256, 128, and 64 bit).

q. Adjust A5, +B15 for a +960 mV dc ±10 uV output.

4-20. External Reference Adjustments (−03 Option)

4-21. If the A4 assembly is installed, perform the following adjustments:

a. Connect a shorting jumper between the EXT REF input terminals on the rear panel.

b. Call EXT REF, 16V range, and a +15.36V output (8192, 4096, 2048, and 1024 bit).

c. Adjust A4, EXT REF ZERO for a 0 ±10 uV output.

d. Disconnect the jumper from the EXT REF input terminals.

e. Apply a 10V ±1mV ac signal having a frequency of 100 Hz to the EXT REF input terminals. Use an ac voltmeter to verify the amplitude of the 100 Hz ac signal.

f. Reconnect the ac/dc voltmeter to the OUTPUT terminals. Ensure that the ac mode is selected on the voltmeter.

g. Call EXT REF, 16V range and a +10.24V output (8192 and 2048 bit).

h. Adjust A4, EXT REF GAIN for an ac voltmeter reading, at the output, of 10.2400 V ± 1 mV.

i. Call 16V range and a +0V output.

j. Disconnect the ac source from the power source and select the dc mode on the voltmeter.

4-22. Current Limiter Adjustment (–06 Option)

4-23. If the A8 assembly is installed, perform the following adjustments:

a. Call 16V range and a –0V output.

b. Connect a 10 ohm, 20w resistive load between the ±OUTPUT terminals on the power source. Ensure that the ac/dc voltmeter is still connected to the OUTPUT terminals and the dc mode is selected.

c. Call 16V range, current limit of 1A, and a –11V output (8192, 2048, 512, 128, 64, 32, 16, 8 and –SIGN bit for direct coupled logic or 4096, 1024, 256, 8, and –SIGN bit for isolated control logic).

d. Adjust A8, REF for a –10V dc ±25 mV output.

e. Call current limit of 10 mA and adjust A8, –I for a –100 mV dc ±1mV output.

f. Call a +11V output (8192, 2048, 512, 128, 64, 32, 16 and 8 bit) and adjust A8, +I for a +100 mV dc ±1 mV output.

g. Call a current limit of 1A, observing that the output is +10V dc ±250 mV.

h. Call 16V range, +0V output, and disconnect the 10 ohm, 20w load.

4-24. Final Zero Adjustment

4-25. The following adjustments must be performed after a minimum operating period of ½ hour with the dust cover in place.

a. Call 16V range and a +0V output.

b. Adjust A3, ZERO for a 0V ±10 uV output.

c. Call 65V range and a +0V output. The output should be 0V ±30 uV. If necessary, adjust A3, ZERO until the specified results of step a. through c. are obtained.

d. If the A4 assembly (External Reference –03 Option) is installed, call EXT REF, 16V range, and a +15.36V output (8192, 4096, 2048, and 1024 bit).

e. Connect a shorting jumper between the EXT REF input terminals on the rear panel.

f. Adjust A4, EXT REF ZERO for a 0V ±10 uV output.

g. Call 16V range, +0V output, and disconnect the jumper from the EXT REF input terminals.

4-26. Output Checks

a. Perform the 16V range linearity checks in Table 4-3, observing that the specified outputs are obtained.

b. If the A4 External Reference assembly (–03 Option) is installed, call 16V range and a +0V output.

c. Apply a 10V ac signal having a frequency of 30 kHz to the EXT REF input terminals. Record the input signal level with the ac/dc voltmeter used to monitor the power source output.

d. Reconnect the ac/dc voltmeter to the OUTPUT terminals. Ensure that the ac mode is selected.

e. Call EXT REF, 16V range, and a +10.24V output (8192 and 2048 bit). The output should be 10.24V ±3V.

g. Turn off the power source and disconnect the test equipment.

f. Call EXT REF, 65V range and a +10.24 output (256 bit). The output should be 10.24V ±3 V.

h. Install the top dust cover. Calibration is complete and the power source is ready for operation.

Table 4-3. LINEARITY CHECKS

CALLED OUTPUT (16V RANGE)		POWER SOURCE OUTPUT VOLTAGE (VDC)	CALLED OUTPUT (16V RANGE)		POWER SOURCE OUTPUT VOLTAGE (VDC)
SIGN (POLARITY)	BINARY CODE		SIGN (POLARITY)	BINARY CODE	
+	0	0 ±10 uV	+	4096	+4.096V ±200 uV
+	64, 4	+68 mV ±40 uV	+	4096, 1024	+5.12V +250 uV
+	128, 8	+136 mV ±40 uV	+	4096, 2048	+6.144V ±300 uV
+	128, 64, 8, 4	+204 mV ±40 uV	+	4096, 2048, 1024	+7.168V ±350 uV
+	256, 16, 1	+273 mV ±50 uV	+	8192	+8.192V ±400 uV
+	256, 64, 16, 4, 1	+341 mV ±50 uV	+	8192, 1024	+9.216V ±450 uV
+	256, 128, 16, 8, 1	+409 mV ±50 uV	+	8192, 2048	+10.24V ±500 uV
+	256, 128, 64, 16, 8, 4, 1	+477 mV ±50 uV	+	8192, 4096, 2048, 1024, 512, 256, 128, 64, 32, 16, 8, 4, 2, 1	+16.383V ±1 mV
+	512, 32, 2	+546 mV ±50 uV			
+	512, 64, 32, 4, 2	+614 mV ±50 uV			
+	512, 128, 32, 8, 2	+682 mV ±50 uV	−	1	−16.383V ±1 mV
+	1024	+1.024V ±50 uV			
+	2048	+2.048V ±100 uV			
+	2048, 1024	+3.072V ±150 uV			

Section 5
List of Replaceable Parts

5-1. INTRODUCTION

5-2. This section contains an illustrated parts breakdown list of the instrument and a Cross Reference List of FLUKE stock numbers to original MANUFACTURERS' part numbers. It also lists recommended spare parts and contains part ordering information. The starting page number of each major listing is given in the Table of Contents.

5-3. The parts list shows the location of all assemblies and the replaceable components. Major assemblies are identified by a designation beginning with the letter A followed by a number (e.g., A1 etc). Subassemblies are identified in the same manner; however, the parent assembly designator precedes this designator (e.g., A1A1 etc.). Electrical components are identified by their schematic diagram designator and listed hardware parts are identified by the FLUKE stock number. All listed components are described, and the FLUKE stock number is given. The original MANUFACTURER'S part number for each listed item is given in the Cross Reference List at the rear of this section.

5-4. PARTS LIST COLUMN DESCRIPTIONS

a. The REF DESIG column indexes the item description to the associated illustration. In general the reference designations are listed under each assembly in alpha-numeric order. Subassemblies of minor proportions are sometimes listed with the assembly of which they are a part. In this case, the reference designations may appear out of order.

b. The DESCRIPTION column describes the salient characteristics of the component. Indention of the description indicates the relationship to other assemblies, components, etc. In many cases it is necessary to abbreviate in this column. For abbreviations and symbols used, refer to Appendix B located at the rear of the manual.

c. The six-digit part number, by which the item is identified at the John Fluke Mfg. Co., Inc. is listed in the STOCK NO. column. Use this number when ordering parts from the factory or authorized representatives. In the case where a flag note is used, special ordering is required. Flag note explanations are located as close as possible to the flag note.

d. The TOT QTY column lists the total quantity of the item used in each particular assembly. This quantity reflects only the latest Use Code. Second and subsequent listings of the same item are referenced to the first listing with the abbreviation REF.

e. Entries in the REC QTY column indicate the recommended number of spare parts necessary to support one to five instruments for a period of two years. This list presumes an availability of common electronic parts at the maintenance site. For maintenance for one year or more at an isolated site, it is recommended that at least one of each assembly in the instrument be stocked. In

the case of optional subassemblies, plug-ins, etc. that are not always part of the instrument, or are deviations from the basic instrument model, the REC QTY column lists the recommended quantity of the item in that particular assembly.

f. The USE CODE column identifies certain parts which have been added, deleted or modified during the production of the instrument. Each part for which a Use Code has been assigned may be identified with a particular instrument serial number by consulting the Serial Effectivity List, paragraph 5-9. Sometimes when a part is changed, the new part can and should be used as a replacement for the original part.

5-5. MANUFACTURERS' CROSS REFERENCE LIST COLUMN DESCRIPTIONS

a. The six-digit part number, by which the item is identified at the John Fluke Mfg. Co., Inc. is listed in the FLUKE STOCK NO. column. Use this number when ordering parts from the factory or authorized representatives.

b. The Federal Supply Code for the item manufacturer is listed in the MFG column. An abbreviated list of Federal Supply Codes is included in Appendix A.

c. The part number which uniquely identifies the item to the original manufacturer is listed in the MFG PART NO. column. If a component must be ordered by description, the type number is listed.

5-6. HOW TO OBTAIN PARTS

5-7. Standard components have been used whenever possible. Standard components may be ordered directly from the manufacturer by using the manufacturer's part number, or parts may be ordered from the John Fluke Mfg. Co., Inc. factory or authorized representative by using the FLUKE stock number. In the event the part you order has been replaced by a new or improved part, the replacement will be accompanied by an explanatory note and installation instructions, if necessary.

5-8. You can insure prompt and efficient handling of your order to the John Fluke Mfg. Co., Inc. if you include the following information:

a. Quantity.

b. FLUKE Stock Number.

c. Description.

d. Reference Designation.

e. Instrument model and serial number.

Example: 2 each, 215897, Transistor, 2N4126 A2A1Q1 & Q2 for 645A, S/N 123.

If you must order structural parts not listed in the parts list, describe the part as completely as possible. A sketch of the part, showing its location to other parts of the instrument is helpful.

5-9. SERIAL NUMBER EFFECTIVITY

5-10. A Use Code column is provided to identify certain parts that have been added, deleted or modified during production of the Model 4265A. Each part for which a use code has been assigned may be identified with a particular instrument serial number by consulting the Use Code Effectivity List below. All parts with no code are used on all instruments with serial numbers above 123.

USE CODE	SERIAL NUMBER EFFECTIVITY

REF DESIG	DESCRIPTION	STOCK NO	TOT QTY	REC QTY	USE CODE
	BINARY PROGRAMMABLE POWER SOURCE Figure 5-1	4265A			
A1	Mother PCB Assembly (Figure 5-2)	302232	1		
A2	Power Supply PCB Assembly (Figure 5-3)	302307	1		
A3	Pre-Amplifier PCB Assembly (Figure 5-4)	302547	1		
A4	External Reference PCB Assembly (–03 Option) (Figure 5-5)	292581	1		
A5	Binary Ladder PCB Assembly (Figure 5-6)	292524	1		
A6	Isolated Control Logic PCB Assembly (–01 Option) (Figure 5-7)	302539	1		
A6	Direct Coupled Control Logic (–04 Option) (Figure 5-8)	302281	1		
A7	Binary Display PCB Assembly (–02 Option) (Figure 5-9)	302521	1		
A7	No-Display PCB Assembly (–05 Option) (Figure 5-10)	302356	1		
A8	Current Limit PCB Assembly (–06 Option) (Figure 5-11)	302331	1		
A9	Power Ampl. PCB Assembly (Figure 5-6) (Figure 5-12)	302315	1		
A10	Connector PCB Assembly (Figure 5-7) (Figure 5-13)	325068	1		
	Connector, programming, male, 50 contact	307017	1		
	Cover, bottom	308122	1		
	Cover, Top	308072	1		
	Foot	292870	4		
	Line Cord with plug	284174	1		
	Panel, rear	302042	1		
	Panel, front	302034	1		
	Decal, front panel (–02 Option)	312348	1		
	Decal, front panel (–05 Option)	312330	1		
	ACCESSORIES (Not included with the instrument. Order separately).				
	Mating Connector, for programming input lines	266056			
	Rack Mounting Brackets	M04-200-306			
	Manual Control Unit	A4200			

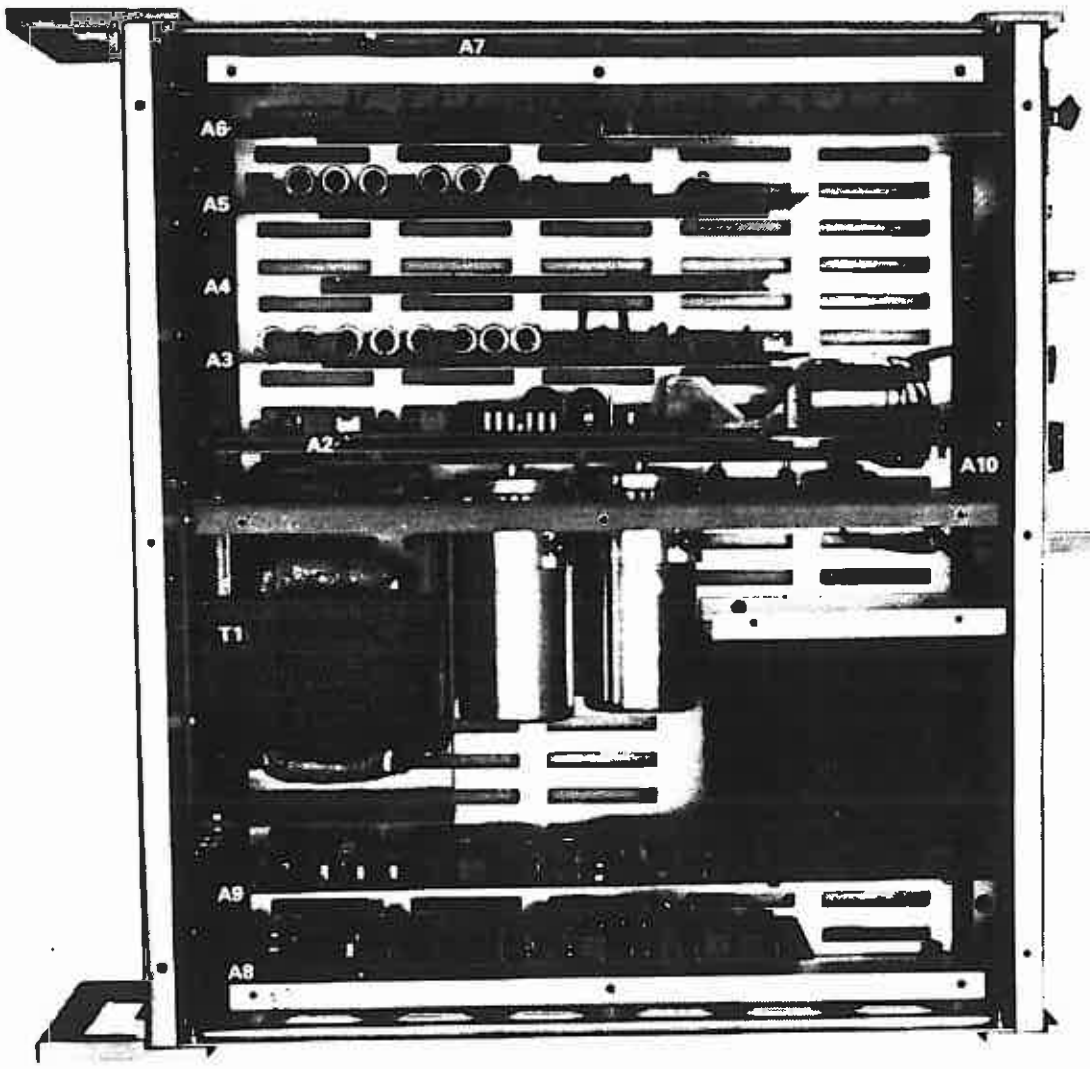


Figure 5-1. MODEL 4265A BINARY PROGRAMMABLE POWER SOURCE

REF DESIG	DESCRIPTION	STOCK NO	TOT QTY	REC QTY	USE CODE
A1	MOTHER PCB ASSEMBLY Figure 5-2	302232	REF		
J1 thru J7	Connector, female, 50 contact	284604	7		

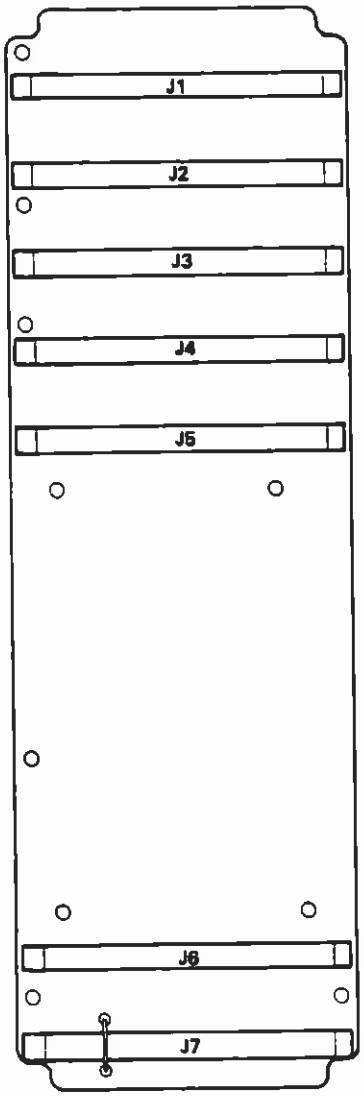


Figure 5-2. MOTHER PCB ASSEMBLY

REF DESIG	DESCRIPTION	STOCK NO	TOT QTY	REC QTY	USE CODE
A2	**POWER SUPPLY PCB ASSEMBLY - Figure 5-3**	302307	REF		
C1, C14, C17	Cap, cer, 0.05 uf +80/−20%, 25v	148924	3		
C2, C5, C9, C10, C19,	Cap, mica, 33 pf ±5%, 500v	160317	5		
C3	Cap, mica, 100 pf ±5%, 500v	148494	1		
C4	Not used				
C6	Cap, cer, 500 pf ±10%, 1 kv	105692	1		
C7, C8	Cap, elect, 250 uf +50/−10%, 64v	185850	2		
C11, C12	Cap, elect, 2100 uf +50/−10%, 150v	223172	2		
C13, C16	Cap, elect, 8000 uf +100/−10%, 15v	309245	2		
C15	Not used				
C18	Cap, Ta, 1.0 uf ±20%, 35v	161919	1		
C20	Cap, cer, 2000 pf, gmv, 1 kv	105569	1		
C21	Cap, cer, 0.1 uf +80/−20%, 500v	105684	1		
C22	Cap, plstc, 0.1 uf ±10%, 400v	289744	1		
CR1, CR25, CR26	Diode, silicon, 1 amp, 600 piv	112383	3		
CR2, CR3, CR27 thru CR35	Diode, silicon, 150 ma	203323	11	2	
CR4, CR14, CR19	Diode bridge, 2 amp	296509	3	1	
CR5 thru CR8, CR10 thru CR13, CR15 thru CR18, CR20 thru CR22, CR24	Not used				
CR9, CR23	Diode, zener, 4.3v	180455	2		
F1	Fuse, slow blow, 2 amp, 250v (For 115v operation)	109181	1		
J1	Connector, male, 3 contact, power	284166	1		

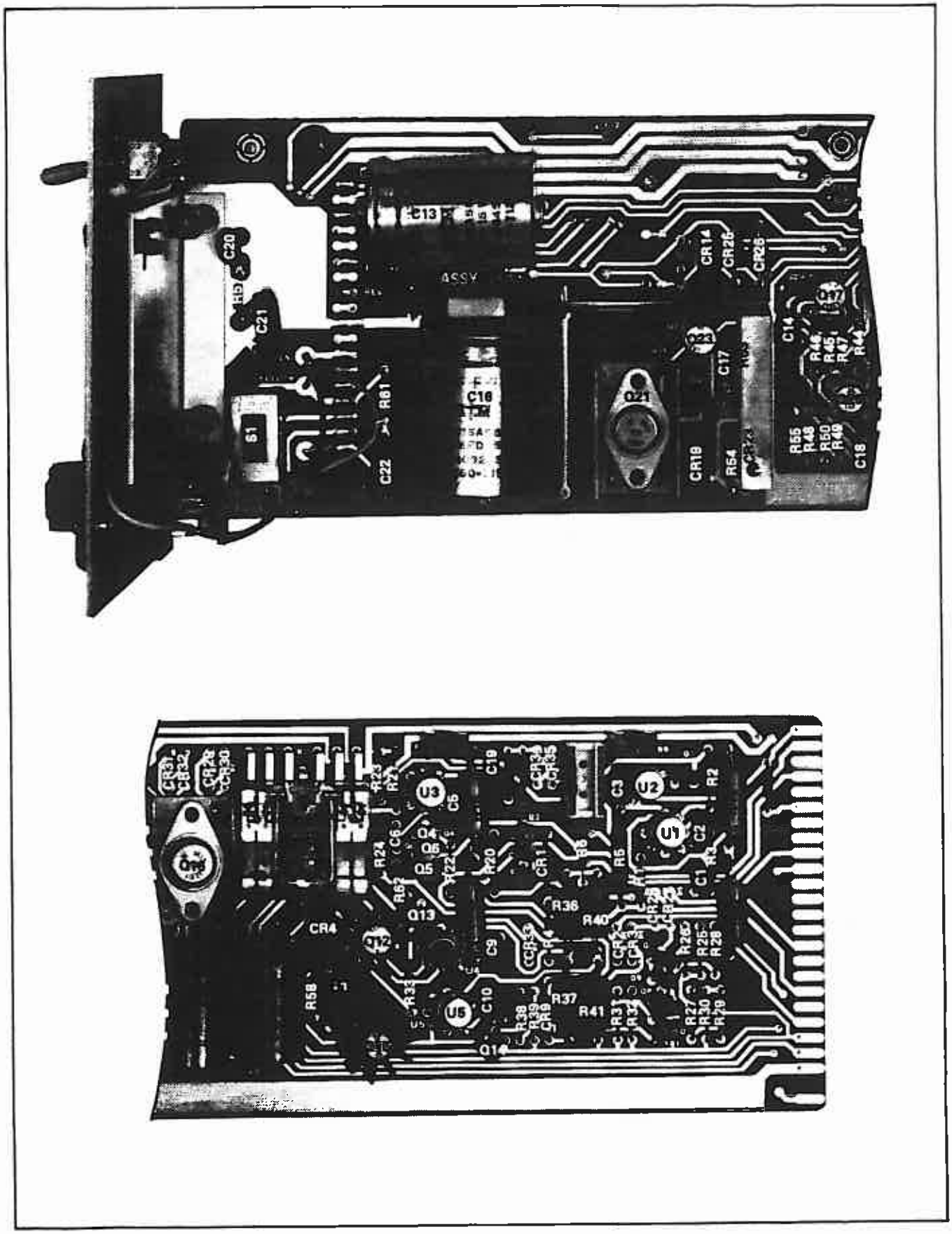
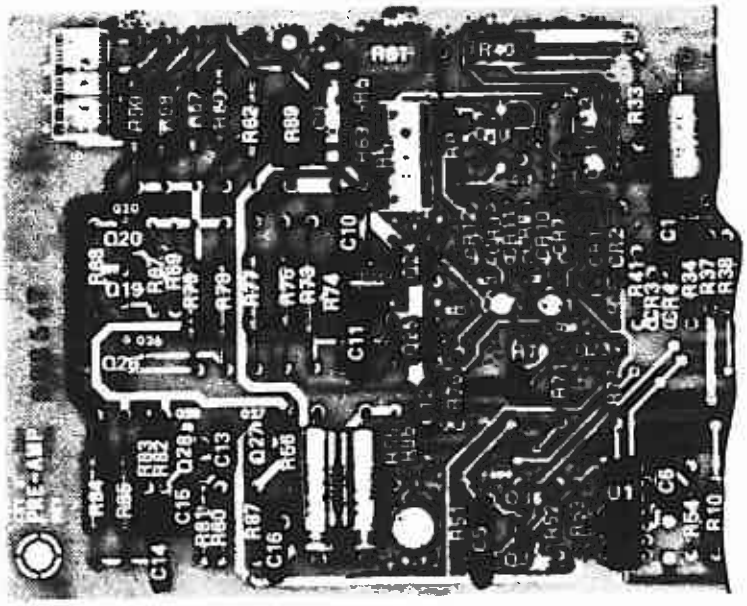


Figure 5-3. POWER SUPPLY PCB ASSEMBLY

REF DESIG	DESCRIPTION	STOCK NO	TOT QTY	REC QTY	USE CODE
J2	Connector, female, 36 contact	285247	1		
K1	Relay, 4PDT, 5v Coil	272716	1	1	
Q1, Q10, Q11, Q13, Q18, Q19, Q24	Tstr, silicon, NPN	218396	7		
Q2, Q3, Q5, Q6	Tstr, J-FET, N-channel	261578	4	2	
Q4, Q7, Q8, Q9, Q14	Tstr, silicon, PNP	195974	5		
Q12, Q17, Q23	Tstr, silicon, NPN	150359	3		
Q15, Q20	Tstr, silicon, PNP	269076	2		
Q16, Q21	Tstr, silicon, NPN	288381	2	1	
Q22	Tstr, J-FET, N-channel	271924	1		
Q25	Tstr, J-FET, N-channel	288324	1	1	
R1, R55	Res, comp, 1k ±5%, 1/4w	148023	2		
R2	Res, met flm, 2.87k ±1%, 1/8w	185629	1		
R3, R46	Res, met flm, 17.4k ±1%, 1/8w	236802	2		
R4	Res, met flm, 5.76k ±1%, 1/8w	260349	1		
R6	Res, met flm, 13.7k ±1%, 1/8w	236752	1		
R7, R8, R22, R24, R28, R30	Res, comp, 22k ±5%, 1/4w	148130	6		
R9	Res, var, cermet, 20Ω ±20%, 1/2w	285114	1		
R10 thru R13	Not used				
R14	Res, met flm, 40.2Ω ±1%, 1/8w	245373	1		
R15	Not used				
R17	Res, ww, 20.02k ±0.1% } Matched Set	291674	1	1	
R18	Res, ww, 20k ±0.1% } Matched Set				
R19	Res, var, cermet, 50Ω ±10%, 1/2w	285122	1		
R20	Res, met flm, 10k ±1%, 1/8w	168260	1		
R21	Res, met flm, 30.1k ±1%, 1/8w	168286	1		

REF DESIG	DESCRIPTION	STOCK NO	TOT QTY	REC QTY	USE CODE
R23, R44	Res, comp, 10k ±5%, 1/4w	148106	2		
R25, R26, R48	Res, comp, 3.9k ±5%, 1/4w	148064	3		
R27, R29	Res, comp, 2k ±5%, 1/4w	202879	2		
R31, R32, R38	Res, comp, 2.7k ±5%, 1/4w	170720	3		
R33, R39	Res, comp, 4.7Ω 5%, 1/4w	193359	2		
R34, R35	Not used				
R36	Res, ww, 10k ±0.1%, 1/4w	240945	1		
R37, R41	Res, ww, 4.02k ±0.1%, 1/4w	240937	2		
R40	Res, ww, 3.74k ±0.1%, 1/4w	246173	1		
R45, R49, R50, R53, R58, R60	Res, comp, 470Ω ±5%, 1/4w	147983	6		
R47	Res, met flm, 3.74k ±1%, 1/8w	272096	1		
R51, R52	Not used				
R54	Res, comp, 22Ω ±5%, 1/2w	169847	1		
R57,R61	Res, comp, 10Ω ±5%, 1/4w	147868	2		
R59	Res, factory selected value, may not be installed				
R62	Res, met flm, 7.15k ±1%,1/8w	260356	1		
S1	Switch, slide, dpdt, line voltage	234278	1		
S2	Switch, toggle, dpdt, power	115113	1		
T1	Transformer, power (See Figure 5-1)	299602	1		
U1	IC, operational amplifier	271502	1		
U2	IC, reference amplifier				
R5	Res, met flm, selected value } Matched Set	301846	1		
R16	Res, ww, 12k ±0.05%, 1/4w } Matched Set				
R56	Res, ww, 1/4w, selected value } Matched Set				
U3	IC, operational amplifier, selected	225961	1		
U4,U5	IC, operational amplifier	321224	2		
TB1	Terminal barrier strip	295212	1		
XF1	Fuse holder	160846	1		
	Socket, IC, 14 contact	276527	1		
	Heat sink, Q12 & Q15	104646	2		
	Jumper, terminal barrier strip	283713	3		

REF DESIG	DESCRIPTION	STOCK NO	TOT QTY	REC QTY	USE CODE
A3	**PRE-AMPLIFIER PCB ASSEMBLY** Figure 5-4	302547	REF		
C1, C5	Cap, mica, 1000 pf ±5%, 500v	148387	2		
C2, C6, C12	Cap, mica, 330 pf ±5%, 500v	148445	3		
C3	Not used				
C4	Cap, mica 33 pf ±5%, 500v	160317	1		
C7, C8	Cap, elect, 20 uf +25/−10%, 50v	106229	2		
C9	Cap, elect, 50 uf +50/−10%, 25v	168823	1		
C10	Cap, mica, 3600 pf ±2%, 500v	176644	1		
C11	Cap, mica, 3300 pf ±2%, 500v	192518	1		
C13	Cap, mica, 150 pf ±5%, 500v	148478	1		
C14, C16	Cap, cer, 0.05 ±20%, 100v	149161	2		
C15	Cap, mica, 22 pf ±5%, 500v	148551	1		
CR1, CR2, CR5, CR6	Diode, silicon, 75 ma, 90 piv	260554	4		
CR3, CR4, CR7 thru CR12	Diode, silicon, 150 ma	203323	8		
Q1, Q2, Q3, Q6, Q7, Q10, Q11, Q14, Q15, Q31, Q32	Tstr, FET-SET, N-channel	256487	11		
Q4, Q8, Q12, Q16, Q34, Q37	Tstr, silicon, PNP	195974	6		
Q5, Q9, Q13, Q17, Q19, Q20, Q26, Q33, Q36	Tstr, silicon, NPN	218396	9		
Q18	Tstr, FET, dual, N-channel, selected	225987	1		
Q21, Q22, Q35	Tstr, FET, P-channel	306142	3		
Q23	Tstr, silicon, NPN	159855	1		
Q24, Q25	Tstr, silicon, PNP, dual	242016	2		
Q27, Q28	Tstr, silicon, NPN	269084	2		



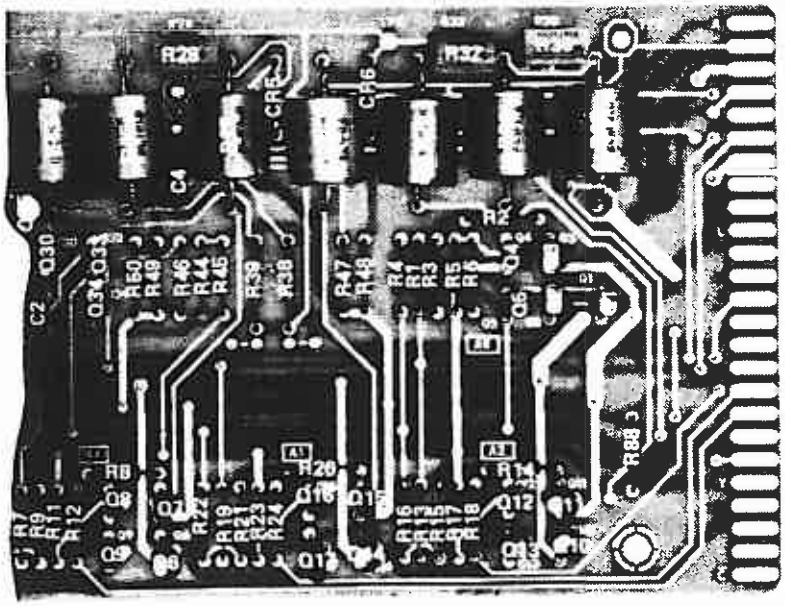


Figure 5-4. MODEL 4265A PRE-AMPLIFIER PCB ASSEMBLY

REF DESIG	DESCRIPTION		STOCK NO	TOT QTY	REC QTY	USE CODE
Q29	Tstr, silicon, NPN		150359	1		
Q30	Tstr, J-FET, N-channel		288324	1		
R1, R3, R7, R9, R13, R15, R19, R21, R38, R41	Res, comp, 51k ±5%, 1/4 w		193334	10		
R2, R8, R14, R20, R47, thru R50, R70	Res, comp, 100k ±5%, 1/4w		148189	9		
R4, R6, R10, R12, R16, R18, R22, R24, R44, R46	Res, comp, 2.7k ±5%, 1/4w		170720	10		
R5, R11, R17, R23	Res, comp, 560 Ω ±5%, 1/4w		147991	4		
R25	Res, ww, 187.6k ±0.1%, 1/2w					
R26	Res, ww, 25.013k ±0.1%, 1/2w					
R27	Res, ww, 50k ±0.1%, 1/2w					
R29	Res, ww, 100.025k ±0.1%, 1/2w	Matched Set	296095	1		
R31	Res, ww, 200 .075k ±0.1%, 1/2w					
R35	Res, ww, 80.08k ±0.1%, 1/2w					
R42, R43	Res, ww, 13.328k ±0.1%, 1/2w					
R28, R40	Res, var, cermet, 50Ω ±5%, 1w		285122	2		
R30	Res, var, cermet, 100Ω ±10%, 1w		285130	1		
R32	Res, var, cermet, 200Ω ±10%, 1w		285148	1		
R33	Res, met flm, 4.02k ±1%, 1/8w		235325	1		
R34	Res, met flm, 12.1k ±1%, 1/8w		234997	1		
R36	Res, met flm, 1.922k ±1%, 1/8w		296343	1		
R37	Res, comp, 100m ±10%, 1/2w		190520	1		
R39	Res, met flm, 641Ω ±1%, 1/8w		296335			
R45	Res, comp, 1k ±5%, 1/4w		148023	1		
R51	Res, comp, 1.5k ±5%, 1/4w		148031	1		

REF DESIG	DESCRIPTION	STOCK NO	TOT QTY	REC QTY	USE CODE
R52, R53, R83, R86, R88	Res, comp, 5.1k ±5%, 1/4w	193342	5		
R54	Res, met flm, 40.2k ±1%, 1/8w	235333	1		
R55, R56, R63, R87	Res, comp, 10Ω ±5%, 1/4w	147868	1		
R57	Res, met flm, 187k ±1%, 1/8w	296376	1		
R58	Res, met flm, 374k ±1%, 1/2w	262105	1		
R59	Res, met flm, 750k ±1%, 1/2w	155192	1		
R60	Res, met flm, 1.27M ±1%, 1/2w	229252	1		
R61	Res, var, cermet, 100k ±10%, 1w	288308	1		
R62	Res, met flm, 107k 1%, 1/2w	296384	1		
R64, R65	Res, ww, 6.8k ±0.03%, 1/2w	254359	2		
R67, R69	Res, met flm, 2k ±1%, 1/8w	277137	2		
R68	Res, met flm, 10k ±1%, 1/8w	291633	1		
R71	Res, comp, 22k ±5%, 1/4w	148130	1		
R72	Res, comp, 10k ±5%, 1/4w	148106	1		
R73, R75	Res, met flm, 49.9k ±1%, 1/2w	182980	2		
R74	Res, met flm, 2.1k ±1%, 1/2w	193276	1		
R76, R80	Res, comp, 100Ω ±5%, 1/4w	147926	2		
R77, R84	Res, met flm, 10k ±1%, 1/2w	151274	2		
R78, R85	Res, met flm, 4.87k ±1%, 1/2w	247775	2		
R79	Res, met flm, 2.49k ±1%, 1/2w	193995	1		
R81	Res, comp, 910Ω ±5%, 1/4w	203851	1		
R82	Res, comp, 680Ω ±5%, 1/4w	148007	1		
R89	Res, ww, 45Ω ±1%, 1/8w	111815	1		
U1	IC, TTL, Monostable Multivibrator	293050	1		
	Socket, IC, 14 contact	276527	2		

REF DESIG	DESCRIPTION	STOCK NO	TOT QTY	REC QTY	USE CODE
A4	**EXTERNAL REFERENCE PCB ASSEMBLY (−03 OPTION) - Figure 5-5**	292581	REF		
C1, C3	Cap, elect, 20 uf +75/−10%, 50v	106229	2		
C2	Cap, mica, 390 pf ±5%, 500v	148437	1		
C4, C6	Cap, mica, 82 pf ±5%, 500v	148502	2		
C5	Cap, mica, 270 pf ±5%, 500v	148452	1		
C7, C11	Cap, cer, 0.05 uf ±20%, 100v	149161	2		
C8, C9	Cap, mica, 5 pf ±10%, 500v	148577	2		
C10	Cap, mica, 22 pf ± 5%, 500v	148551	1		
CR1 thru CR4	Diode, silicon, 150 ma	203323	4		
Q1	Tstr, J-FET, dual, N-channel, selected	225987	1		
Q2, Q3, Q6, Q12	Tstr, silicon, NPN	218396	4		
Q4, Q5	Tstr, silicon, PNP, dual	242016	2		
Q7, Q8	Tstr, silicon, NPN	269084	2		
Q9, Q10	Tstr, J-FET, N-channel	261578	2		
Q11	Tstr, silicon, PNP	195974	1		
Q13, Q14	Tstr, silicon, NPN	150359	2		
R1 R16	Res, ww, 100.025k Res, ww, 99.955k } Matched Set	291682	1		
R2, R11	Res, comp, 10Ω ±5%, 1/4w	147868	2		
R3, R4	Res, ww, 6.8k ±0.03%, 1/2w	254359	2		
R5	Res, met flm, 107k ±1%, 1/2w	296384	1		
R6	Res, var, cermet, 100k ±10%, 1/2w	288308	1		
R7	Res, met flm, 1.27M ±1%, 1/2w	229252	1		
R8	Res, met flm, 750k ±1%, 1/2w	155192	1		
R9	Res, met flm, 374k ±1%, 1/2w	262105	1		
R10	Res, met flm, 187k ±1%, 1/2w	296376	1		
R12	Res, ww, 45Ω ±0.1%, 1/8w	111815	1		
R13, R15	Res, met flm, 2k ±1%, 1/8w	277137	2		

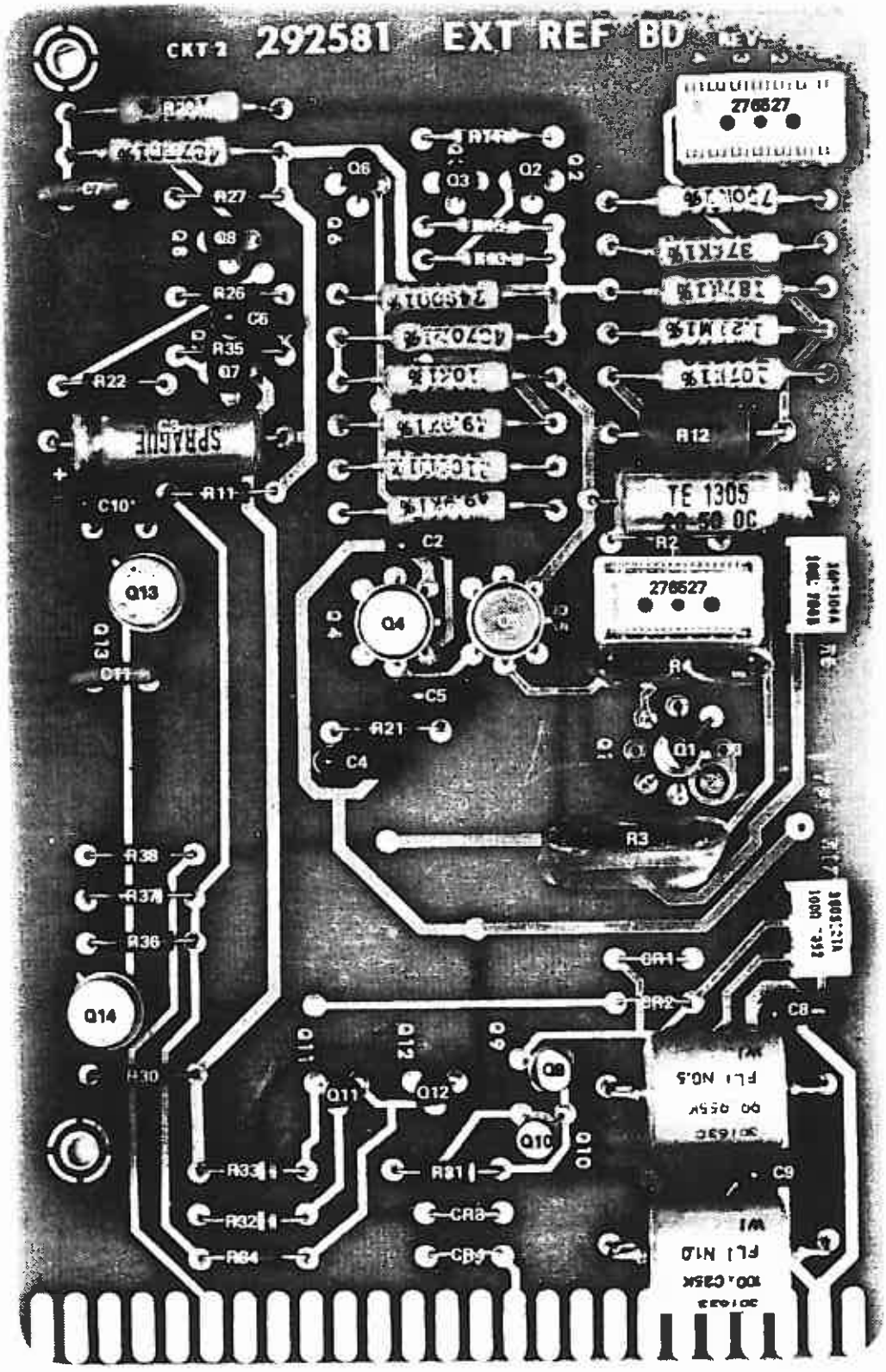


Figure 5-5. EXTERNAL REFERENCE PCB ASSEMBLY (–03 EXTERNAL REFERENCE OPTION)

REF DESIG	DESCRIPTION	STOCK NO	TOT QTY	REC QTY	USE CODE
R14	Res, met flm, 10k ±1%, 1/8w	291633	1		
R17	Res, var, cermet, 100Ω ±10%, 1/2w	285130	1		
R18, R20	Res, met flm, 49.9k ±1%, 1/2w	182980	2		
R19	Res, met flm, 2.1k ±1%, 1/2w	193276	1		
R21, R35	Res, comp, 100Ω ±5%, 1/4w	147926	2		
R22	Res, comp, 5.1k ±5%, 1/4w	193342	1		
R23, R28	Res, met flm, 10k ±1%, 1/2w	151274	2		
R24, R29	Res, met flm, 4.87k ±1%, 1/2w	247775	2		
R25	Res, met flm, 2.49k ±1%, 1/2w	193995	1		
R26	Res, comp, 1k ±5%, 1/4w	148023	1		
R27, R36	Res, comp, 820Ω ±5%, 1/4w	148015	2		
R30	Res, comp, 18k ± 5%, 1/4w	148122	1		
R31	Res, comp, 47k ±5%, 1/4w	148163	1		
R32, R33	Res, comp, 3.9k ±5%, 1/4w	148064	2		
R34	Res, comp, 2.7k ±5%, 1/4w	170720	1		
R37	Res, comp, 4.7k ±5%, 1/4w	148072	1		
R38	Res, comp, 270Ω ±5%, 1/4w	160812	1		
	Socket, IC, 14 contact	276527	2		

REF DESIG	DESCRIPTION	STOCK NO	TOT QTY	REC QTY	USE CODE
A5	**BINARY LADDER PCB ASSEMBLY—Figure 5-6**	292524	REF		
C1, C2	Cap, cer, 0.05 uf ±20%, 100v	149161	2		
CR1	Diode, silicon, 150 ma	203323	1		
Q1	Diode, Field Effect, current regulator	285106	1		
Q2	Tstr, silicon, NPN	168716	1		
Q7,Q11,Q15, Q19,Q23,Q27, Q31,Q35,Q47, Q51	Tstr, silicon, NPN	218396	10	2	
Q3	Tstr, silicon, PNP	269076	1		
Q4,Q37 thru Q44	Not used				
Q5,Q9,Q13, Q17,Q21,Q25 Q29,Q33,Q45 Q49	Tstr, silicon, PNP	195974	10	2	
Q6, Q8	Tstr, J-FET, N-channel, U2366E, Matched Pair	306399	1		
Q10, Q12	Tstr, J-FET, N-channel, U2366E, Matched Pair	306381	1		
Q14,Q16,Q18 Q20	Tstr, J-FET, N-channel, U2366E, Matched Pairs (Q14 matched to Q16; Q18 matched to Q20)	306373	2		
Q22,Q24,Q26 Q28,Q30,Q32 Q34,Q36	Tstr, J-FET, N-channel, U2366E, Matched Set	298307	1		
Q46,Q48,Q50 Q52	Tstr, FET, N-channel	261578	4	1	
R1	Res, var, cermet, 500Ω ±10%, 1w	291120	1		
R2	Res, ww, 24.987k ±0.1%	296111	1		
R3	Res, ww, 50k ±0.1%				
R5	Res, ww, 100.025k ±0.1%				
R6	Res, ww, 200.07k ±0.1%				
R7	Res, ww, 187.6k ±0.1%				
	Matched Resistor Set				
R4,R16, R17,R18,R21, R22,R71 thru R82	Not used				
R8	Res, met flm, 2.94k ±1%, 1/8w	261628	1		

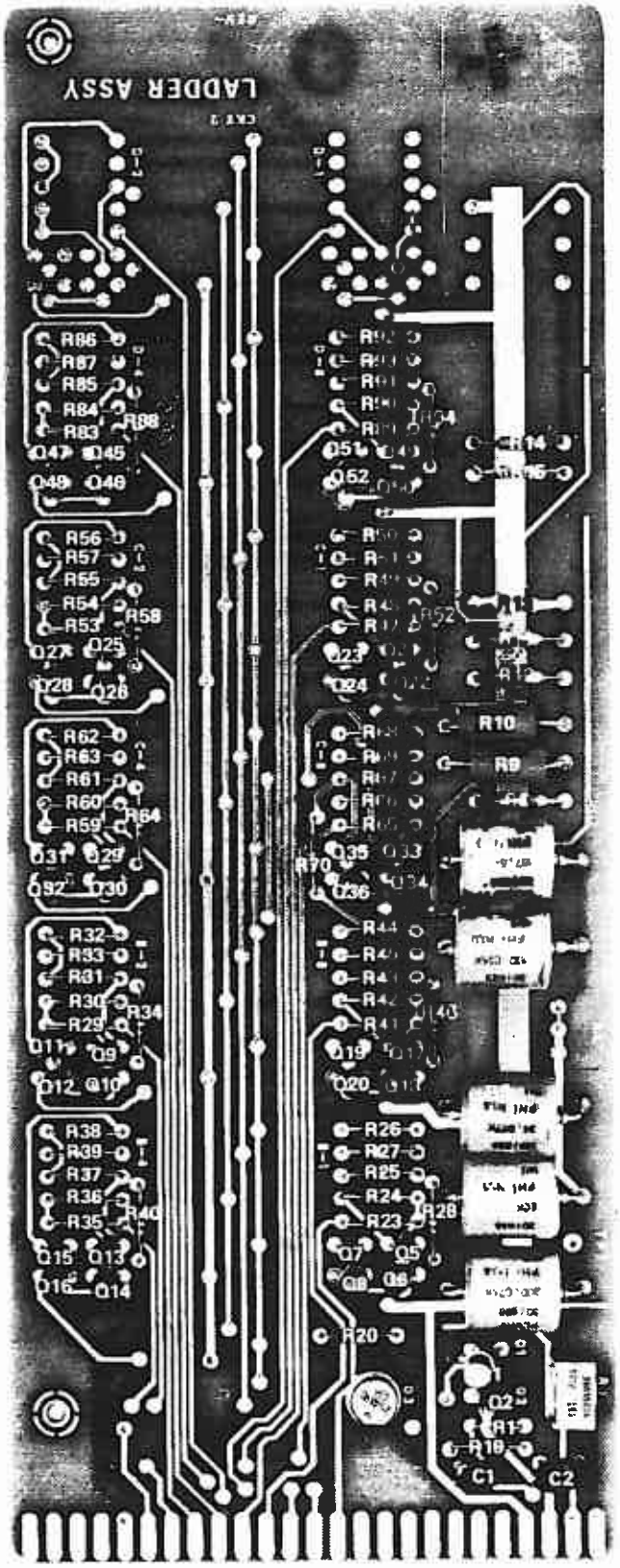


Figure 5-6. BINARY LADDER PCB ASSEMBLY

REF DESIG	DESCRIPTION	STOCK NO	TOT QTY	REC QTY	USE CODE
R9	Res, ww, 24.987k ±0.03%, 1/4w	289769	1		
R10	Res, ww, 50k ±0.03%, 1/4w	289777	1		
R11	Res. met flm, 100.03k ±0.1%, 1/8w	291088	1		
R12, R13	Res. met flm, 200.08k ±0.1%, 1/8w	290122	2		
R14	Res, met flm, 200k ±1%, 1/8w	261701	1		
R15	Res, met flm, 100k ±1%, 1/8w	291054	1		
R19	Res, comp, 1.8k ±5%, 1/4w	175042	1		
R24,R30,R36, R42,R48,R54, R60,R66,R84, R90	Res, comp, 560Ω ±5%, 1/4w	147991	10		
R20	Res, comp, 20k ±5%, 1/4w	221614	1		
R25,R27,R28, R31,R33,R34, R37,R39,R40, R43,R45,R46, R49,R51,R52, R55,R57,R58, R61,R63,R64, R67,R69,R70, R85,R87,R88, R91,R93,R94	Res, comp, 51k ±5%, 1/4w	193334	30		
R23,R26,R29, R32,R35,R38, R41,R44,R47, R50,R53,R56, R59,R62,R65 R68,R83,R86, R89,R92	Res, comp, 2.7k ±5%, 1/4w	170720	20		

REF DESIG	DESCRIPTION	STOCK NO	TOT QTY	REC QTY	USE CODE
A6	**LOGIC ASSEMBLY** Figure 5-7	331801	REF		
C1	Cap, plstc. 0.001μf ±10%, 200V	159582	1		
C2, C3	Cap, mica, 12 pf ±5%, 500V	175224	2		
C4, C47	Cap, mica, 100 pf ±1%, 500V	226126	2		
C5	Cap, Ta, 0.68μf ±10%, 35V	182790	1		
C6	Cap, plstc, 3300 pf ±2%, 100V	168344	1		
C7, C8, C9, C29, C50	Cap, mica, 56 pf ±5%, 500V	148528	5		
C10	Cap, mica, 270 pf ±5%, 500V	148452	1		
C11 thru C25, C28, C34 thru C40, C43 thru C46	Cap, cer, 0.025μf ±20%, 50V	168435	27		
C26, C42	Cap, elect, 200μf ±50/−10%, 10V	236935	2		
C27	Cap, cer, 2700 pf gmv, 600V	106211	1		
C30	Cap, mica, 620 pf ±5%, 500V	215244	1		
C31, C49	Cap, mica, 360 pf ±1%, 500V	170407	2		
C32	Cap, mica, 220 pf ±5%, 500V	170423	1		
C33	Cap, plstc, 0.1μf ±10%, 50V	271866	1		
C41	Not used				
C48	Cap, plstc, 0.0075μf ±2%, 100V	168369	1		
CR3, CR4	Diode, high-speed switch	256339	2		
CR5 thru CR9	Diode, Si, 150 mA	203323	5		
Q1, Q3 thru Q15	Xstr, Semicon, Si, NPN	159855	1		
Q2, Q16	Xstr, unijunction, Si	268110	2		
R1	Res, met flm, 523Ω ±1%, 1/8w	294835	1		
R2, R13, R23, R24, R27, R29, R31, R33, R41, R44, R46, R50	Res, comp, 1k ±5%, 1/4w	148023	12		
R3	Res, comp, 2.7Ω ±5%, 1/4w	246744	1		
R4	Res, comp, 1.5k ±5%, 1/4w	148031	1		

REF DESIG	DESCRIPTION	STOCK NO	TOT QTY	REC QTY	USE CODE
R5, R6, R7	Not used				
R8	Res, met flm, 11.5k ±1%, 1/8w	267138	1		
R9, R54	Res, comp, 100k ±5%, 1/4w	148189	2		
R10, R55	Res, comp, 390k ±5%, 1/4w	193383	2		
R11, R58	Res, comp, 390Ω ±5%, 1/4w	147975	2		
R12	Res, comp, 1.3k ±5%, 1/4w	234252	1		
R14	Res, met flm, 32.4k ±1%, 1/8w	182956	1		
R15	Res, comp, 12k ±5%, 1/4w	159731	1		
R16, R37 thru R40, R42, R60	Res, comp, 200Ω ±5%, 1/4w	193482	7		
R17, R21, R25, R51	Res, comp, 510Ω ±5%, 1/4w	218032	4		
R18, R36, R45, R47, R48, R49, R50	Res, comp, 3.3k ±5%, 1/4w	148056	7		
R19, R20	Res, met flm, 6.98k ±1%, 1/8w	261685	2		
R22, R26, R28, R30, R32, R43	Res, comp, 51Ω ±5%, 1/4w	221879	6		
R34, R52, R56	Res, met flm, 10k ±1%, 1/8w	168260	3		
R35	Not used				
R53	Res, met flm 28k ±1%, 1/8w	291385	1		
R57	Res, comp, 27k ±5%, 1 4w	148148	1		
R61	Res, comp, 5.1k ±5%, 1/4w	193342	1		
T1 thru T6	Xfmr, pulse	299594	6		
U1, U2	IC, TTL, MSI, Eight-Input Multiplexer	326165	2		
U3, U16	IC, TTL, Hex Inverter	293076	2		
U4	IC, TTL, Digital, Multiplexer	288852	1		
U5	IC, TTL, 4-Bit Up-Down Counters	293183	1		
U6, U26	IC, TTL, Hex Inverter	292979	2		
U7	IC, TTL, J-K Flip-Flop	296491	1		
U8, U17	IC, TTL, Dual Retriggerable Monostable Multivibrator	310235	2		

REF DESIG	DESCRIPTION	STOCK NO	TOT QTY	REC QTY	USE CODE
U9	IC, TTL, Dual 2-Wide 2-Input AND/OR Gate	293084	1		
U10	IC, TTL, J-K Flip-Flop, AND Inputs	293092	1		
U11	IC, TTL, Quad, 2-Input, Pos AND Gates	292987	1		
U12	IC, TTL, Quad, 2-Input Nand Gate	292953	1		
U13, U14	IC, TTL, Dual Peripheral Positive Nand Driver	329706	2		
U15, U18	IC, TTL, Monostable Multivibrator	293050	2		
U19	IC, TTL, Retriggerable Monostable Multivibrator	293134	1		
U20, U21, U22	IC, TTL, 8-Bit Shift Register	272138	3		
U23	IC, TTL, MSI, Dual 4-Bit Latch	293191	1		
	Conn, female, 50 contact	267252	1		

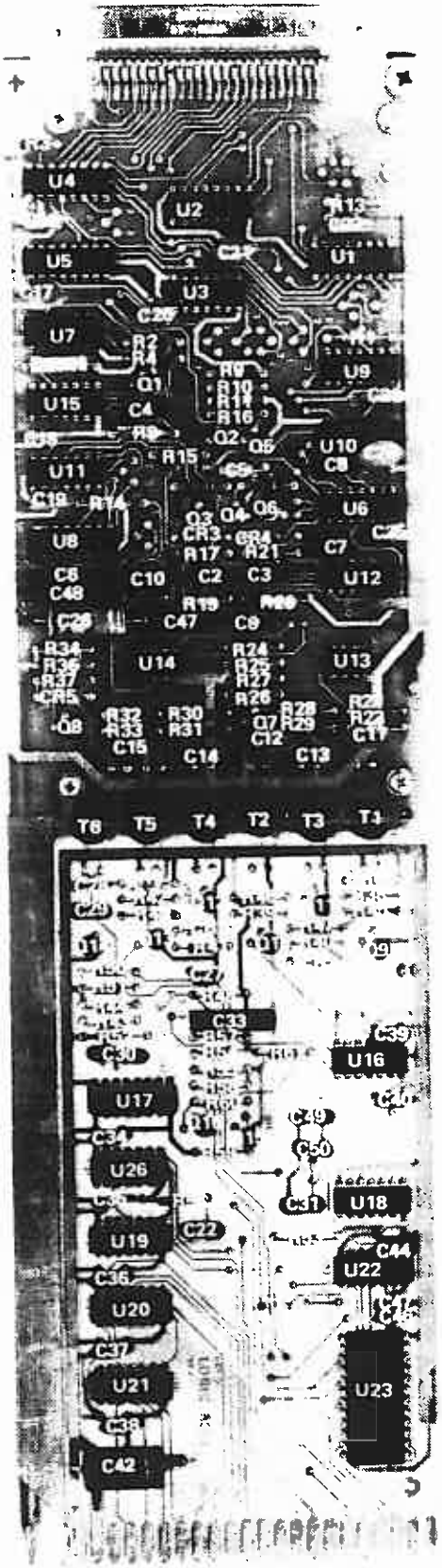


Figure 5-7. ISOLATED CONTROL LOGIC

REF DESIG	DESCRIPTION	STOCK NO	TOT QTY	REC QTY	USE CODE
A6	**DIRECT COUPLED CONTROL LOGIC (–04 OPTION)** **Figure 5-8**	302281	REF		
C1	Cap, plstc, .01 uf ±2%, 100v	168385	1		
C2, C3	Cap, elect, 200 uf +50/–10%, 10v	236935	2		
CR1 thru CR26	Diode, zener, 5.6v	277236	26	2	
J1	Connector, female, 50 contact	267252	1		
Q1 thru Q28	Tstr, silicon, NPN	159855	28		
R1	Res, met flm, 32.4k ±1%, 1/8w	182956	1		
R2	Res, comp, 1k ±5%, 1/4w	148023	1		
R3	Res, comp, 390Ω ±5%, 1/4w	147975	1		
R4, R7, R10, R13, R16, R19, R22, R25, R28, R31, R34, R37, R40, R43, R46, R49 R52, R55, R58, R61, R64, R67, R70, R73, R76, R80, R85	Res, comp, 3.3k ±5%, 1/4w	148056	27		
R5, R8, R11, R14, R17, R20, R23, R26, R29, R32, R35, R38, R41, R44, R47, R50, R53, R56, R59, R62, R65, R68, R71, R74, R77, R81, R84	Res, comp, 1.5k ±5%, 1/4w	148031	27		
R6, R9, R12, R15, R18, R21, R24, R27, R30, R33, R36, R39, R42, R45, R48, R51, R54, R57, R60, R63, R66, R69, R72, R75, R78, R82	Res, comp, 470Ω ±5%, 1/4w	147983	26		
R83	Res, comp, 2.7Ω ±5%, 1/4w	246744	1		
U1	IC, TTL, Quad 2-Input NAND Gate	292953	1		
U2	IC, TTL, Hex Inverter	292979	1		
U3	IC, TTL, Retriggerable Monostable Multivibrator	293134	1		

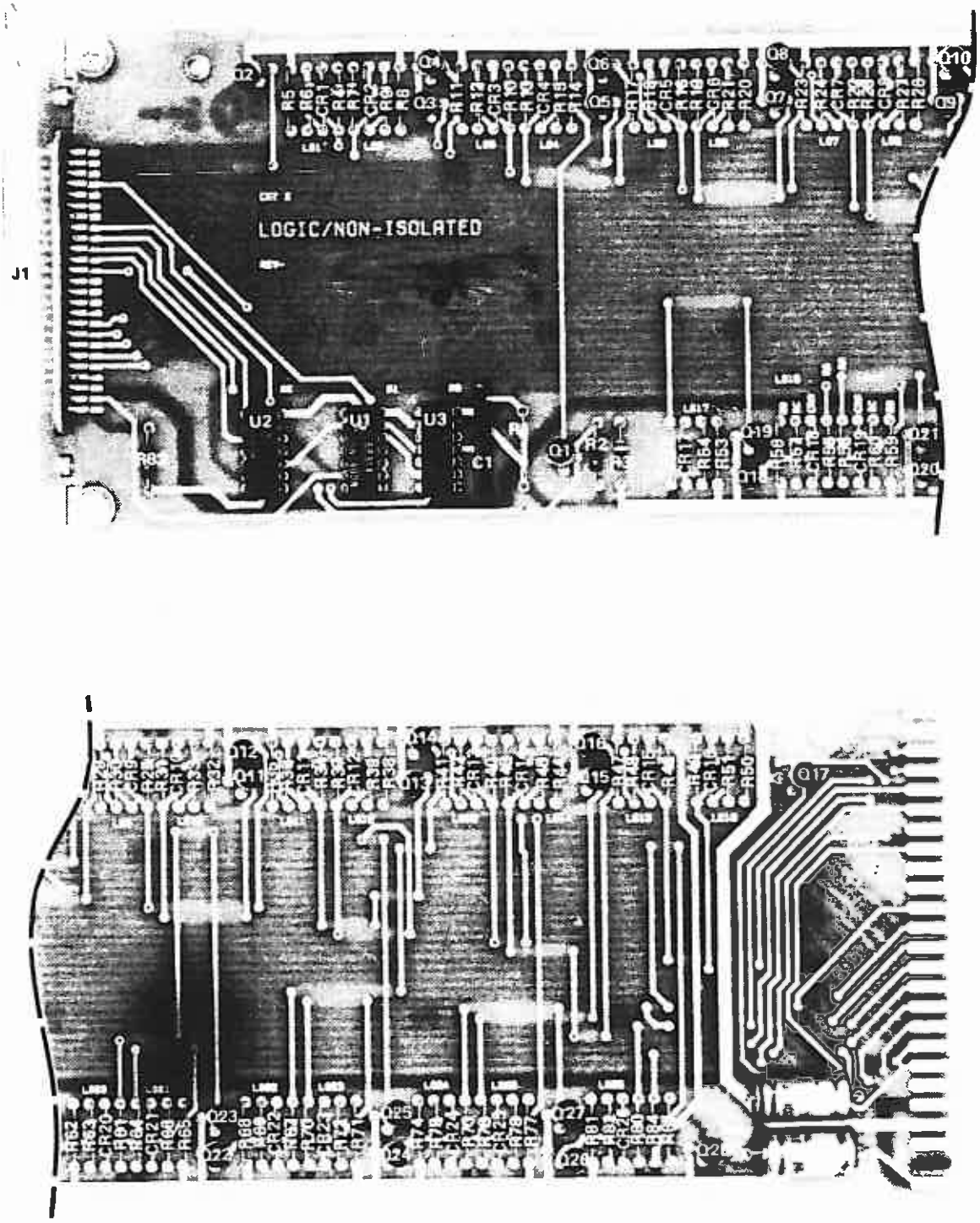


Figure 5-8. NON ISOLATED LOGIC PCB ASSEMBLY (–04 DIRECT COUPLED CONTROL OPTION)

REF DESIG	DESCRIPTION	STOCK NO	TOT QTY	REC QTY	USE CODE
A7	**DISPLAY BCD PCB ASSEMBLY** **Figure 5-8**	302257	REF		
CR1 thru CR27	Diode, light emitting	309617	27		
R1 thru R27	Res, comp, 270Ω ±5%, 1/4w	160804	27		
U1 thru U5	IC, TTL, Hex Inverter	292979	5		

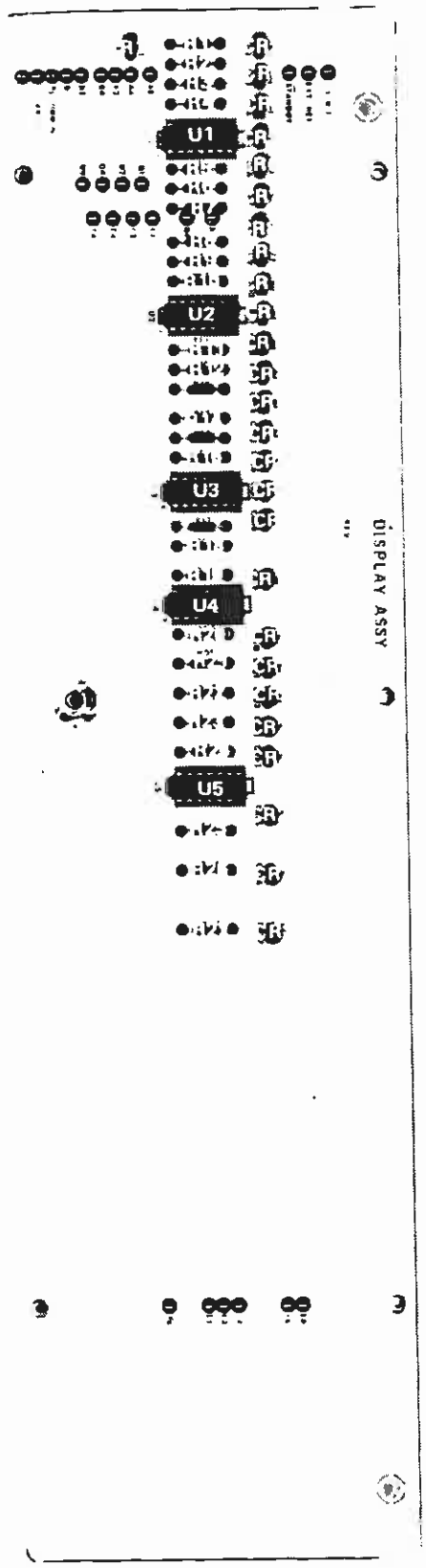


Figure 5-9. BINARY DISPLAY PCB ASSEMBLY (–02 FRONT PANEL DISPLAY OPTION)

REF DESIG	DESCRIPTION	STOCK NO	TOT QTY	REC QTY	USE CODE
A7	**NO DISPLAY PCB ASSEMBLY (–05 OPTION)** **Figure 5-10**	302356	REF		
CR1	Diode, light emitting	309617	1		
R1	Res, comp, 270Ω ±5%, 1/4w	160804	1		

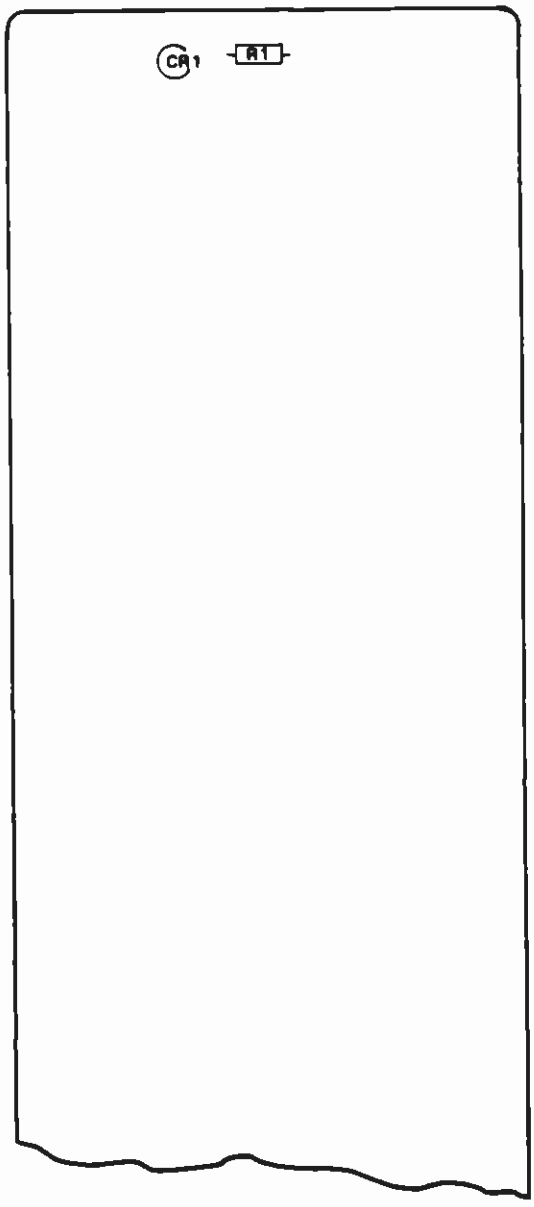


Figure 5-10. NO DISPLAY PCB ASSEMBLY (–05 OPTION)

REF DESIG	DESCRIPTION	STOCK NO	TOT QTY	REC QTY	USE CODE
A8	**CURRENT LIMIT PCB ASSEMBLY (–06 Option)** **Figure 5-11**	302331	REF		
C1, C2 C12	Cap, plstc, 0.1 uf ±10%, 250v	161992	3		
C3	Cap, mica, 10 pf ±10%, 500v	175216	1		
C4, C5	Cap, plstc, 0.033 uf ±10%, 100v	106062	2		
C6	Cap, mica, 4 pf ±5%, 500v	190397	1		
C7	Cap, mica, 27 pf ±5%, 500v	177998	1		
C8, C9, C13 thru C16	Cap, cer, 0.0012 uf ±10%, 500v	106732	6		
C10, C11	Cap, mica, 33 pf ±5%, 500v	160317	2		
C17	Cap, plstc, 0.022 uf ±10%, 250v	234484	1		
CR1, CR2	Diode, zener, 16v	113332	2		
CR3, CR5, CR10, CR11	Diode, zener, 3.9v	113316	4		
CR4, CR8	Diode, zener, 8v	246611	2		
CR6, CR9	Diode, zener, 36v	186163	2		
CR7	Diode, zener, 6.3v, 7.5 mA	172148	1		
Q1, Q2, Q5 Q8, Q11, Q14, Q16, Q19, Q20	Tstr, silicon, NPN	218396	9		
Q3, Q7, Q10, Q13, Q15, Q21, Q23	Tstr, silicon, PNP	195974	7		
Q4, Q6, Q9, Q12, Q26	Tstr, J-FET, N-channel	261578	5		
Q17	Tstr, semicon, silicon, PNP, dual	242016	1		
Q18	Tstr, silicon, PNP	276899	1		
Q22	Tstr, silicon, PNP	284448	1		
Q24, Q27, Q28	Tstr, silicon, NPN	218511	3		
Q25	Tstr, silicon, NPN, dual	220087	1		

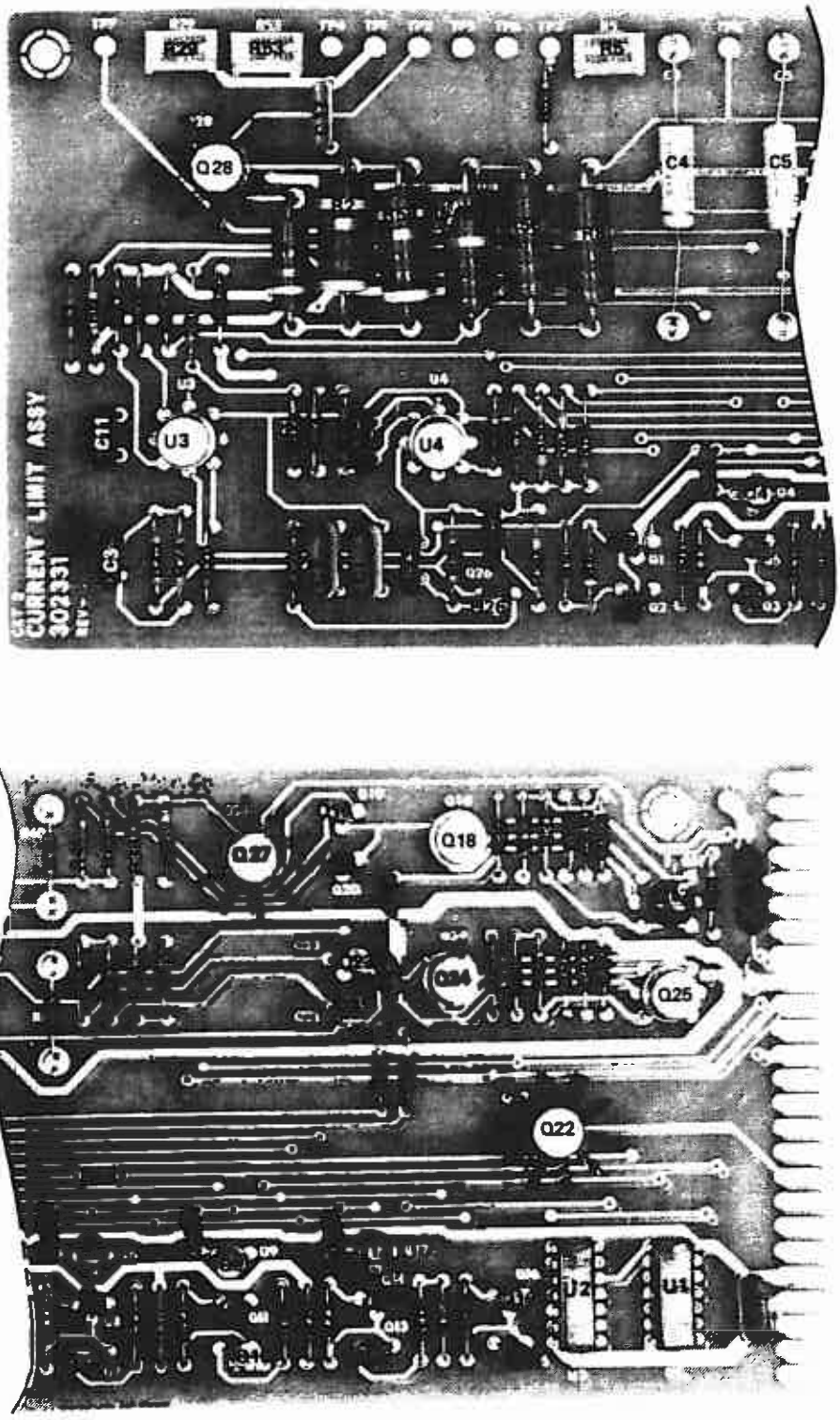


Figure 5-11. CURRENT LIMIT PCB ASSEMBLY (–06 OPTION)

REF DESIG	DESCRIPTION	STOCK NO	TOT QTY	REC QTY	USE CODE
R1	Res, comp, 24k ±5%, 1w	275644	1		
R2, R58	Res, comp, 4.7k ±10%, 2w	245308	2		
R3	Res, met film, 649Ω ±1%, 1/8w	309955	1		
R4	Res, met film, 750Ω ±1%, 1/8w	312801	1		
R5	Res, var, cermet, 500Ω ±10%, 1w	291120	1		
R6	Res, met film, 15Ω ±1%, 1/8w	296434	1		
R7, R56, R57	Res, comp, 1.8k ±10%, 2w	185983	3		
R8	Res, comp, 47k ±5%, 1/4w	148163	1		
R9	Res, comp, 10k ±5%, 1/4w	148106	1		
R10, R12, R16, R19, R22	Res, comp, 24k ±5%, 1/4w	193425	5		
R11, R13, R17, R21, R23, R33	Res, comp, 12k ±5%, 1/4w	159731	6		
R14, R18, R20, R32, R50	Res, comp, 27k ±5%, 1/4w	148148	5		
R15, R54	Res, met film, 6.19k ±1%, 1/8w	283911	2		
R24, R25	Res, met film, 10k ±1%, 1/8w	168260	2		
R26, R35	Res, comp, 5.1M ±5%, 1/4w	296467	2		
R27	Res, comp, 5.1k ±5%, 1/4w	193342	1		
R28, R34	Res, comp, 10M±5%, 1/4w	194944	2		
R29, R53	Res, var, cermet, 20k ±10%, 1/2w	291609	2		
R30, R52	Res, met film, 24.9k ±1%, 1/8w	291369	2		
R31	Res, met film, 2.74k ±1%, 1/8w	293761	1		
R36, R49	Res, comp, 24K ±5%, 1/2w	108654	2		
R37, R48	Res, comp, 36k ±5%, 1/4w	221929	2		
R38, R46	Res, comp, 39k ±5%, 1/4w	188466	2		
R39, R47	Res, comp, 22k ±5%, 1/4w	148130	2		
R39, R47	Res, comp, 33k ±5%, 1/2w	108761	2		
R40, R45	Res, comp, 120Ω ±5%, 1/4w	170712	2		

REF DESIG	DESCRIPTION	STOCK NO	TOT QTY	REC QTY	USE CODE
R41, R44, R59	Res, comp, 1.2k ±5%, 1/4w	190371	3		
R42, R43	Res, comp, 100Ω ±5%, 1/4w	147926	2		
R51	Res, ww, 1Ω ±1%, 2w	229534	1		
R55	Res, met film, 12.4k ±1%, 1/8w	261644	1		
R60, R61, R62	Res, comp, 56Ω ±5%, 1/4w	147900			
U1, U2	IC, DTL, Hex Inverter	268367	2		
U3, U4	IC, Operational amplifier	271502	2		

REF DESIG	DESCRIPTION	STOCK NO	TOT QTY	REC QTY	USE CODE
A9	**POWER AMPL. PCB ASSEMBLY** **Figure 5-12**	302315	REF		
C1, C4	Cap, mica, 330 pf ±1%, 500v	226142	2		
C2, C3	Cap, mica, 33 pf ±5%, 500v	160317	2		
C5, C9, C10, C16, C22	Cap, mica, 100 pf ±5%, 500v	148494	5		
C6	Cap, mica, 68 pf ±5%, 500v	148510	1		
C7, C15	Cap, elect, 10 uf +50/−10%, 150v	106351	2		
C8	Cap, elect, 125 uf +50/−10% ,16v	186296	1		
C11, C13, C21	Cap, plstc, 0.47 uf ±10%, 250v	184366	3		
C12, C14 C17, C18, C19, C20	Not used				
C23	Cap, mica, 150 pf ±5%, 500v	148478	1		
C24, C25	Cap, plstc, 0.022 uf ±10%, 250v	234484	2		
C26, C27	Cap, cer, 0.01 uf ±20%, 100v	149153	2		
C28, C29	Cap, mica, 10 pf ±10%, 500v	175216	2		
CR1 thru CR10,CR12, CR13,CR19 thru CR22, CR31,CR32, CR35 thru CR37	Diode, silicon, 150 mA	203323	21		
CR11, CR17	Not used				
CR14,CR16, CR24,CR25, CR27 thru CR30,CR33, CR34,CR38, CR39	Diode, silicon, 1 amp, 600 piv	112383	12		
CR18	Diode, zener, 36v	237354	1		
CR23, CR26	Diode, zener, 36v	186163	2		
P1 thru P8	Connector, receptacle	267633	8		
Q1	Tstr, silicon, PNP	266619	1		

REF DESIG	DESCRIPTION	STOCK NO	TOT QTY	REC QTY	USE CODE
Q2, Q3, Q4, Q8, Q11, Q13, Q18, Q20 thru Q26, Q29, Q38	Tstr, silicon, NPN	218511	16		
Q5, Q6, Q7, Q9, Q10, Q12, Q14, Q17, Q30, Q36	Tstr, silicon, PNP	284448	10		
Q15, Q27, Q28, Q35	Tstr, silicon, PNP	195974	4		
Q16, Q19, Q34, Q39, Q40	Tstr, silicon, NPN	218396	5		
Q31	Tstr, silicon, NPN	190710	1		
Q32, Q33, Q41, Q42	Tstr, silicon, NPN, power, (on heat sink)	313213	4		
Q37	Tstr, silicon, PNP, power	309302	1		
R1, R2, R9 R10, R23	Res, comp, 2k ±5%, 1/4w	202879	5		
R3, R8, R69, R73	Res, comp, 20k ±5%, 1/4w	221614	4		
R4, R6	Res, comp, 62k ±5%, 1/4w	220053	2		
R5, R7	Res, comp, 270Ω ±5%, 1/4w	160804	2		
R11	Res, met flm, 1.21k ±1%, 1/8w	229146	1		
R12, R26, R65, R67	Res, comp, 1k ±5%, 1/4w	148023	4		
R13, R31, R40	Res, comp, 100Ω ±5%, 1/4w	147926	3		
R14, R18	Res, comp, 240k ±5%, 1/4w	218016	2		
R15, R19, R63	Res, comp, 330k ±5%, 1/4w	192948	3		
R16, R17	Res, comp, 6.2k ±5%, 1/4w	221911	2		
R20, R22	Res, comp, 10k ±5%, 1/4w	148106	2		
R21	Res, met flm, 10k ±1%, 1/8w	168260	1		
R24	Res, met flm, 6.04k ±1%, 1/8w	285189	1		
R25	Res, met flm, 30.1k ±1%, 1/8w	168286	1		
R27	Res, comp, 1.8k ±5%, 1w	180331	1		

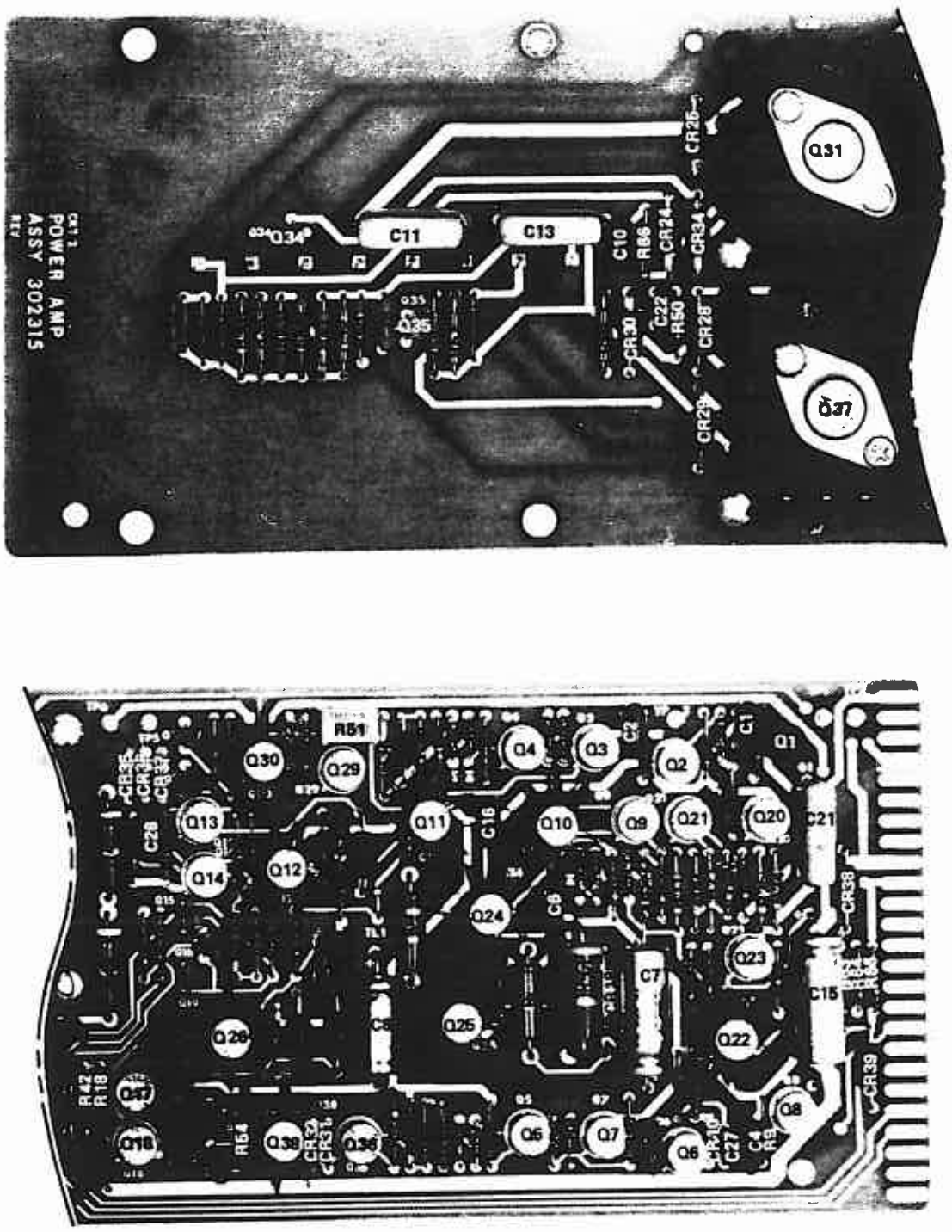


Figure 5-12. POWER AMPLIFIER PCB ASSEMBLY (Sheet 1 of 2)

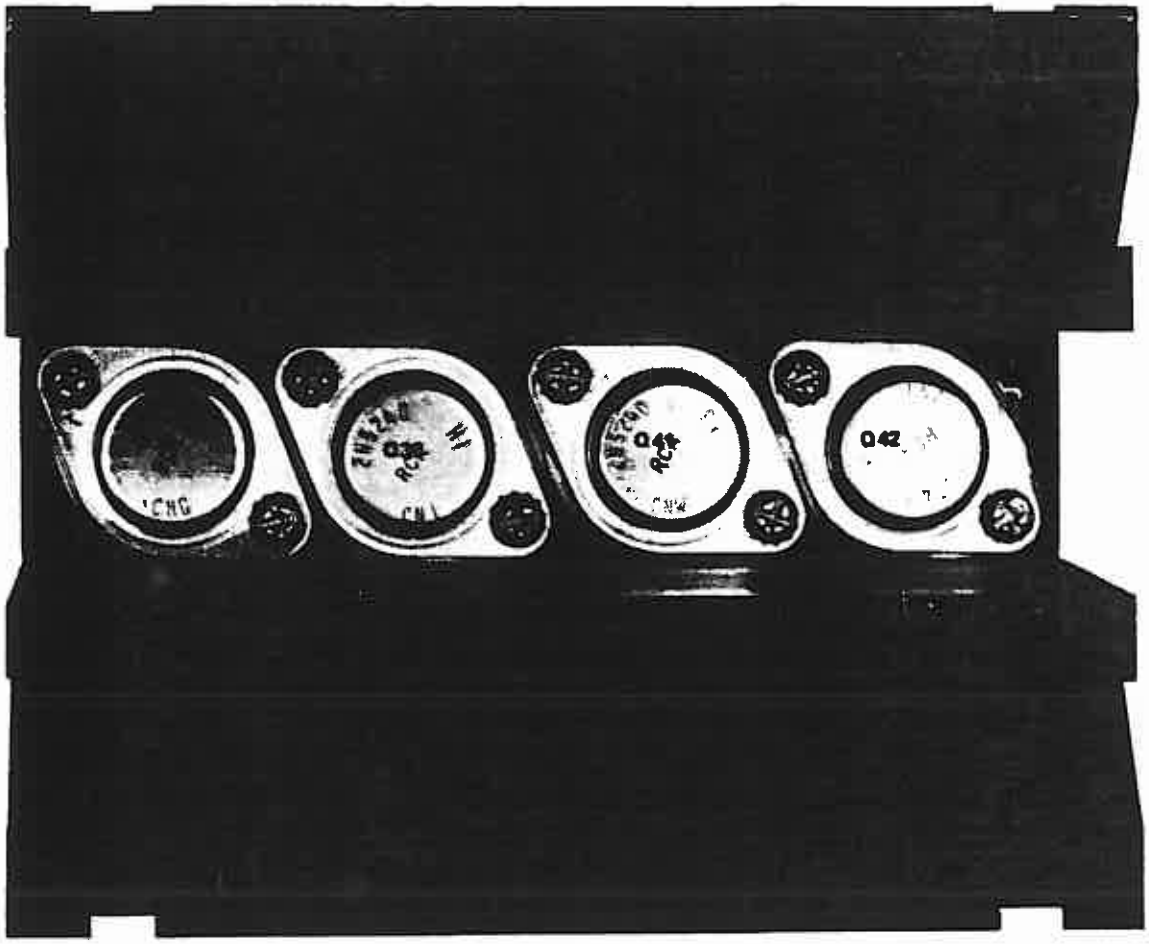


Figure 5-12. POWER AMPLIFIER PCB ASSEMBLY (Sheet 2 of 2)

REF DESIG	DESCRIPTION	STOCK NO	TOT QTY	REC QTY	USE CODE
R28, R29	Res, comp, 180Ω ±5%,1/4w	147942	2		
R30	Res, comp, 13k ±5%, 1w	309641	1		
R32, R55	Res, met flm, 549Ω ±1%, 1/8w	289272	2		
R33, R54	Res, met flm, 100Ω ±1%, 1/8w	168195	2		
R34, R52	Res, met flm, 32.4k ±1%, 1/8w	182956	2		
R35, R59	Res, comp, 15k ±5%, 1/4w	148114	2		
R36, R50, R60, R61, R68, R70, R71, R72	Res, comp, 100k ±5%, 1/4w	148189	8		
R37, R53	Res, comp, 68Ω ±5%, 1/4w	147918	2		
R38, R39, R56, R57	Res, comp, 1Ω ±5%, 1/2w	218693	4		
R41, R46	Res, comp, 4.7k ±10%, 1w	109587	2		
R42, R45	Res, comp, 36Ω ±5%, 1/4w	312843	2		
R43, R44, R47, R48	Res, comp, 1.1Ω ±5%, 1/4w	163717	4		
R49	Res, comp, 51Ω ±5%, 1/2w	144717	1		
R51	Res, var, cermet 100Ω ±10%, 1w	285130	1		
R58	Res, comp, 3.3k ±5%, 2w	218859	1		
R62	Res, met flm, 40.2k ±1%, 1/8w	235333	1		
R64, R66	Res, comp, 1M ±5%, 1/4w	182204	2		
	Connector, receptacle	267617	8		

REF DESIG	DESCRIPTION	STOCK NO	TOT QTY	REC QTY	USE CODE
A10	CONNECTOR PCB ASSEMBLY	325068	REF		
CR1 thru CR4	Diode, silicon, 1 amp, 600 piv	112383	4		
R1, R2	Res, comp, 15k ±10%, 2w	110080	2		

MANUFACTURERS' CROSS REFERENCE LIST

FLUKE STOCK NO.	MFR.	MFR. PART NO.
A4200	89536	A4200
104646	05820	NF207
105569	71590	PA140-139CB
105684	56289	41C92
105692	71590	2DDH60N501K
106062	56289	33392
106229	56289	30D206G05CC4
106351	56289	30D397F150DD4
106674	56289	C023B102G332M
106732	71590	CF-122
108654	01121	EB2425
108761	01121	EB3325
109181	71400	TYPE MDX
109587	01121	GB4721
110080	01121	HB1531
111815	01686	TYPE R1250
112383	05277	IN4822
113316	07910	IN748
113332	07910	IN966A
115113	95146	MST215N
144717	01121	EB5105
147868	01121	CB1005
147900	01121	CB5605
147918	01121	CB6805
147926	01121	CB1015
147942	01121	CB1825
147975	01121	CB3915
147983	01121	CB4715
147991	01121	CB5615
148007	01121	CB6815
148015	01121	CB8215
148023	01121	CB1025
148031	01121	CB1525
148056	01121	CB3325
148064	01121	CB3925
148072	01121	CB4725
148106	01121	CB1035
148114	01121	CB1535
148122	01121	CB1835
148130	01121	CB2235
148148	01121	CB2735
148163	01121	CB4735
148189	01121	CB1045
148387	14655	CD19F101J
148437	14655	CD15F391J
148445	14655	CD15F151J
148452	14655	CD15F271J
148478	14655	CD15F330J
148494	14655	CD15F101J
148502	14655	CD15F820J
148510	14655	CD15F680J
148528	14655	CD15F560J
148551	14655	CD15E220J
148577	14655	CD15C050K
148924	72982	5855-Y50-503Z
149153	56289	C023B101F103M
149161	56289	55C23A1
150359	95303	2N3053
151274	91637	TYPE MFF1/2
155192	91637	TYPE MFF1/2
159731	01121	CB1235
159855	07910	CS23030
160317	14655	CD15E330J
160804	01121	CB2715
160812	01121	CB2705
160846	75915	342004
161919	56289	196D105X0035
161992	73445	C280AE/A100K

MANUFACTURERS' CROSS REFERENCE LIST

FLUKE STOCK NO.	MFR.	MFR. PART NO.
163717	01121	EB11G5
168195	91637	TYPE MFF1/8
168260	91637	TYPE MFF1/8
168286	91637	TYPE MFF1/8
168385	84171	PE103G
168435	56289	C128B101H253M
168716	07263	S19254
168823	25403	C426ARF50
169847	01121	EB2205
170423	14655	CD15F221J
170712	01121	CB1215
170720	01121	CB2725
172148	03877	IN3496
175042	01121	CB1825
175216	01121	CD15C100K
175224	14655	CD15E120J
176644	14655	CD19F360G
177980	14655	CD15F431J
177998	14655	CD15E270J
180331	01121	GB1825
180406	07910	IN758
180455	07910	IN749A
182204	01121	CB1055
182790	56289	150D684X9035A2
182956	91637	TYPE MFF1/8
182980	91637	TYPE MFF1/8
184366	73445	C280AE/A470K
185629	91637	TYPE MFF1/8
185850	73445	C437ARH250
185983	01121	HB1821
186163	07910	IN974B
186296	73445	C426ARE125
188466	01121	CB3935
190371	01121	CB1225
190397	14655	CD15C040K
190520	01121	EB1071
190710	04713	2N3739
192518	14655	CD19F330G
192948	01121	CB3355
193276	91637	TYPE MFF1/2
193334	01121	CB5135
193342	01121	CB5152
193359	01121	CB47G5
193425	01121	CB2435
193482	01121	CB2015
193995	91637	TYPE MFF1/2
194944	01121	CB1065
195974	04713	2N3906
202879	01121	CB2025
203323	03508	DHD1105
203851	01121	CB9115
203869	01121	CB4315
218016	01121	CB2445
218032	01121	CB5115
218396	04713	2N3904
218511	95303	60994
218693	01121	EB10G5
218859	01121	HB3325
220053	01121	CB6235
220087	GE	12E1516
221614	01121	CB2035
221861	01121	CB1105
221911	01121	CB6225
221929	01121	CB3635

MANUFACTURERS' CROSS REFERENCE LIST

FLUKE STOCK NO.	MFR.	MFR. PART NO.
223172	56289	36D212F150BC2B
225961	89536	225961
225987	89536	225987
226142	14655	CD15F331F
226159	14655	CD19F681F500
229146	91637	TYPE MFF1/8
229252	91637	TYPE MFF1/2
229534	91637	TYPE RS-2C
234252	01121	CB1325
234278	82389	XW1649
234484	73445	C280AE/A22K
234997	91637	TYPE MFF1/8
235325	91637	TYPE MFF1/8
235333	91637	TYPE MFF1/8
235366	91637	TYPE MFF1/8
236752	91637	TYPE MFF1/8
236802	91637	TYPE MFF1/8
236885	13511	225-21821-105
236935	73445	C426ARD200
237008	14655	CD19F221J
237354	04713	1N3033
240937	89536	240937
240945	89536	240945
242016	07263	SE4901
245308	01121	HB4721
245373	91637	TYPE MFF1/8
246173	89536	246173
246611	07910	TYPE 1N961B
246744	01121	CB27G5
247775	91637	TYPE MFF1/2
254359	89536	254359
256339	28480	5082-2900
256487	89536	256487
260349	91637	TYPE MFF1/8
260356	91637	TYPE MFF1/8
260554	07910	CD55105
261578	15818	U2366E
261610	91637	TYPE MFF1/8
261628	91637	TYPE MFF 1/8
261644	91637	TYPE MFF1/8
261685	91637	TYPE MFF1/8
261701	91637	TYPE MFF1/8
262105	91637	TYPE MFF1/2
266056	02660	57-30500
266197	01121	CB1625
266619	07263	2N4888
267252	02660	57-40500
267617	00779	85863-5
267633	00779	86144-1
268110	03508	2N6027
268367	04713	MC836P
269076	95303	2N4037
269084	07910	CS2484
271502	12040	LM301A
271866	06001	75F2R5A104
271924	07910	CFE13041
272096	91637	TYPE MFF1/8
272138	12040	DM8570
272716	24796	R40-E030-1
275644	01121	GB2435
276527	23880	TSA-2900-14W
276899	95303	2N5415
277137	91637	TYPE MFF1/8
277202	14655	CD15E430F
277236	07910	1N752A
283713	71285	422-13-11-013
283911	91637	TYPE MFF1/8
284166	82839	EAC301

MANUFACTURERS' CROSS REFERENCE LIST

FLUKE STOCK NO.	MFR.	MFR. PART NO.
284174	70903	KHS-7041
284448	95303	2N5416
284604	02660	225-22521-110
285106	07910	CRE3021
285114	71450	360S-200B
285122	71450	360S-500A
285130	71450	360S-101A
285148	71450	360S-201A
285189	91637	TYPE MFF1/8
285247	02660	225-21821-103MOD
288308	71450	360S-104A
288324	15818	U1994E
288381	95303	40372
288480	91637	TYPE MFF1/8
288845	01295	SN7402N
289272	91637	TYPE MFF1/8
289744	73445	C280CF/A100K
289769	89536	289769
289777	89536	289777
289827	89536	289827
290106	91637	TYPE MFF1/8
290114	91637	TYPE MFF1/8
290122	91637	TYPE MFF1/8
291054	91637	TYPE MFF1/8
291062	91637	TYPE MFF1/8
291070	91637	TYPE MFF1/8
291088	91637	TYPE MFF1/8
291120	71450	360S-501A
291369	91637	TYPE MFF1/8
291609	71450	360S-203A
291633	91637	TYPE MFF1/8
291674	89536	291674
291682	89536	291682
292524	89536	292524
292581	89536	292581
292870	89536	292870
292953	01295	SN7400N
292979	01295	SN7404N
292995	01295	SN7410N
293050	01295	SN74121N
293068	01295	SN74H00N
293076	01295	SN74H04N
293084	01295	SN74H51N
293092	01295	SN74H102N
293134	07263	U6A960159X
293183	01295	SN7472N
293191	04713	MC8308P
293209	07263	U6B930959X
293761	91637	TYPE MFF1/8
295212	71785	TYPE 140Y
296095	89536	296095
296111	89536	296111
296335	91637	Type MFF1/8
296343	91637	Type MFF1/8
296376	91637	TYPE MFF1/2
296384	91637	TYPE MFF1/2
296434	91637	TYPE MFF1/8
296467	01121	CB5175
296491	01295	SN7472N
296509	09423	FB100
298307	89536	298307
299594	89536	299594
299602	89536	299602
301846	89536	301846
302034	89536	302034
302042	89536	302042
302232	89536	302232
302273	89536	302273
302281	89536	302281

MANUFACTURERS' CROSS REFERENCE LIST

FLUKE STOCK NO.	MFR.	MFR. PART NO.	FLUKE STOCK NO.	MFR.	MFR. PART NO.
302307	89536	302307			
302315	89536	302315			
302331	89536	302331			
302349	89536	302349			
302356	89536	302356			
302521	89536	302521			
302539	89536	302539			
302547	89536	302547			
304410	89536	304410			
304485	89536	304485			
304808	89536	304808			
306142	05397	3N173			
306373	89536	306373			
306381	89536	306381			
306399	89536	306399			
307017	02660	57-30500-3			
308072	89536	308072			
308122	89536	308122			
309245	99392	61C15AS83			
309302	04713	2N5345			
309617	71318	FLV102			
309641	01121	GB1325			
309955	91637	TYPEMFF1/8			
312330	89536	312330			
312348	89536	312348			
312801	91637	TYPEMFF1/8			
312843	01121	CB3615			
313213	95303	2N5240			
321224	34333	SG8178T			
325068	89536	325068			

Option-09

Multi-Strobe Isolated Logic

6-1. INTRODUCTION

6-2. The 4200-09 Multi-Strobe Isolated Logic permits any of the Fluke 4200 Series Programmable Voltage Sources (hereafter referred to as the 4200) to be remotely controlled by a large variety of program sources such as a computer, a system coupler, as well as a Fluke Automatic Test Equipment System. The 4200-09 consists of a pair of printed circuit boards mounted as one assembly and connected together by means of a ribbon-type cable. The entire assembly mounts within the 4200 and is accessed through an opening in the rear panel and a 50-pin connector. Up to eight 4200 series power sources equipped with the –09 option (4200-09) may be connected to and addressed by a single program source.

6-3. Programming the 4200 series voltage sources requires that the program source provide certain information to the 4200-09. Such program information required to generate specific output voltages, includes:

a. Output voltage magnitude.

b. Output voltage range.

c. Output voltage polarity.

d. Current limit magnitude.

e. Strobe pulse (s).

f. Voltage source mainframe address.

g. Operate/Standby signal.

CAUTION!

The Model A4200 MCU is NOT compatible with the –09 option.

6-4. In addition to providing signals to the voltage source, the program source should also have the capability to receive status information from the voltage source. By means of unique voltage source mainframe addresses, the program source can determine the status of any particular voltage source in the system. (Refer to Status Checking for details.)

6-5. CONNECTION TO PROGRAM SOURCE

6-6. Connection of the program source to the 4200 is made by means of an interconnecting cable and a 50-pin connector on the rear panel of the 4200. (Refer to Figure 6-1.) The mating connector used on the interconnecting cable is an Amphenol Blue Ribbon 57-30500, Fluke stock number 266056. Up to eight 4200's may be connected to a single program source as shown in Figure 6-2. The first 4200 connects to the program source interface, the second 4200 connects to the first, the third to the second, etc. The cable assemblies used to connect the 4200's are Fluke Stock Number

6-7. INPUT/OUTPUT SIGNALS

6-8. Details of the interface siganls between the 4200-09 and the program source are listed in the following Tables 6-1 and 6-2. Table 6-2 describes those interface signals between the 4200-09 and a program source interface which communicates in binary format. (Positive-true logic employs +5 volts for a logic 1 and zero volts for a logic 0.)

NOTE!

Not all the signals listed in Tables 6-1 and 6-2 apply to all 4200 series voltage sources. For specific programming requirements, refer to the Programming Information given in Section 2 of the technical manual for the particular model voltage source.

NOTE!

The following paragraphs provide jumpering instructions for the 4200-09. Table 6-3 provides abbreviated jumpering instructions with reference to the appropriate text.

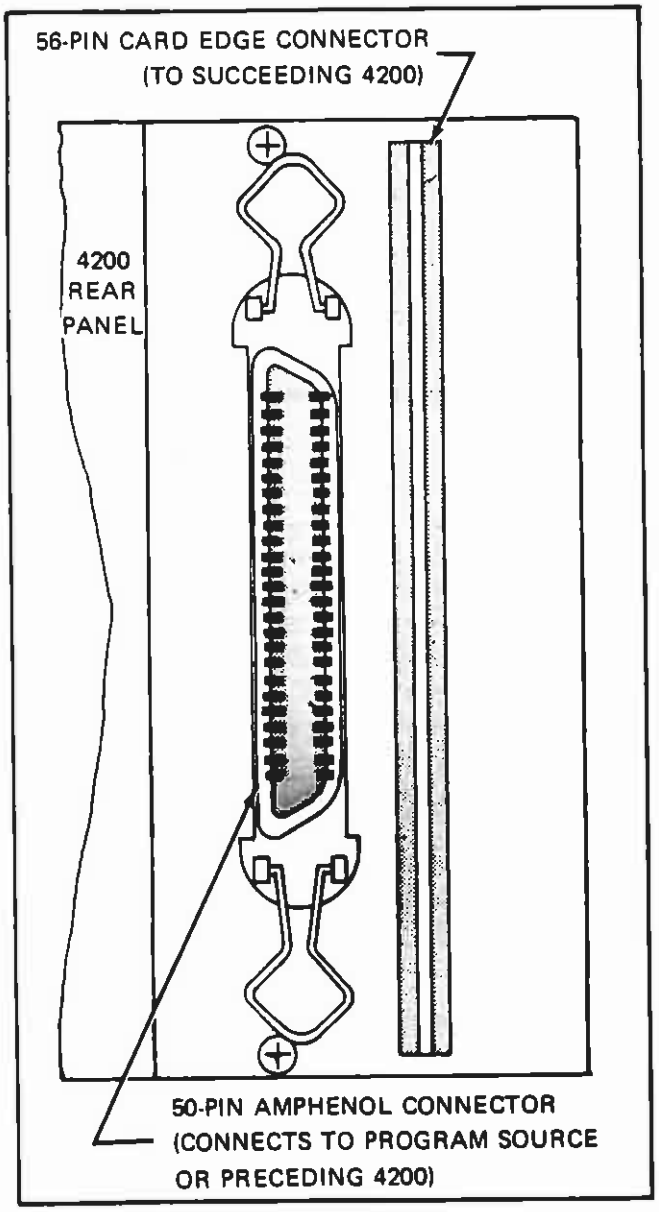


Figure 6-1. 4200-09 CONNECTORS

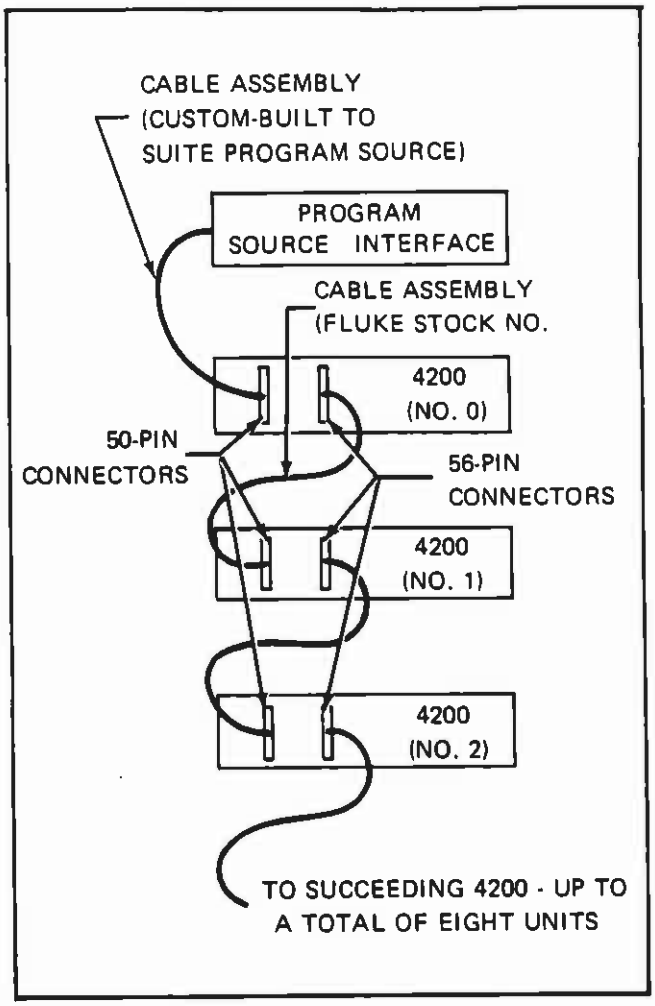


Figure 6-2. MULTIPLE 4200 CONNECTIONS

6-9. DATA WORD/CONTROL WORD LENGTHS

6-10. BCD – Type Voltage Sources

6-11. Program data for BCD-type 4200 voltage sources consists of a 16-bit or a 18-bit data word, and if necessary a control word (up to eight bits in length). Figure 6-3 shows a typical 16-bit data word and an eight-bit control word used to program a BCD-type voltage source. By keeping the four BCD digits of output magnitude data separate from the range, polarity and current limit functions, output voltage can be changed without affecting functions established by a previous control word. To obtain a 16-bit data word and an eight-bit control word, jumper pad T to pad U.

NOTE!

The first bit of the control word may be either the polarity bit or the standby/operate bit. Refer to paragraph 6-22.

Table 6-1. INPUT/OUTPUT SIGNALS, BCD PROGRAM SOURCE (Sheet 1 of 2)

PIN NUMBER		SIGNAL NAME	DESCRIPTION
50 - PIN CONN.	56 - PIN CONN.		
43, 44, 19, & 42	44, 43, 42 & 41	Voltage output magnitude – MSD	Four BCD lines to program the most-significant digit of the output voltage. (Refer also to the schematic diagram for pin number assignments.)
38, 8, 25 & 24	40, 39, 38 & 37	Voltage output magnitude – 2SD	Four BCD lines to program the second most-significant digit of the output voltage.
39, 40, 11 & 10	36, 35 34 & 33	Voltage output magnitude – 3SD	Four BCD lines to program the third most-significant digit of the output voltage.
13, 15, 12 & 14	32, 31, 30 & 29	Voltage output magnitude – LSD	Four BCD lines to program the least significant digit of the output voltage.
26	53	Polarity (Sign)	Single line to program output polarity. Either polarity can be programmed by either logic level as selected by jumpers at PCB pads, W, X, and Y.
1	27	Output Magnitude Range	Single line to program output magnitude range on those voltage sources requiring range selection. (Logic 1 = high range, Logic 0 = low range)
31	55	External Reference	Single line to program external reference mode on those voltage sources equipped with the external reference option. (Logic 1 = ext. reference, Logic 0 = int. reference.)
2	28	Current Limit range	Single line to program range of current output limiting on those voltage sources equipped current limit selection. (Logic 1 = 1 amp range, logic 0 = 100 mA range)
37, 35, 5 & 3	4, 3, 2 & 1	Current Limit Magnitude	Four lines to select the current limit value, expressed as a percentage of the programmed range. Up to 120% can be programmed. Any attempt to program 0% results in 10%. (Refer also to the schematic diagram for pin number assignments.)
17	45	Standby/operate (address zero)	Single line used to select the standby or operate mode of the voltage source. Either mode can be programmed by either logic level as selected by jumpers at PCB pads 18 and 19.
23, 22, 34, 7, 6 & 4	46 thru 52	Standby/operate (addresses one through seven)	Seven lines (through connections) used to select the standby or operate mode of up to seven succeeding voltage sources. (Refer to schematic diagram for pin number assignments.)

Table 6-1. INPUT/OUTPUT SIGNALS, BCD PROGRAM SOURCE (Sheet 2 of 2)

PIN NUMBER		SIGNAL NAME	DESCRIPTION
50 - PIN CONN.	56 - PIN CONN.		
20	12	Instrument mainframe (address zero)	Single line used to address the voltage source in order to perform any programming function. The addressing signal must be present in order for any strobe signal to be recognized by the 4200-09 logic. Addressing may be by either logic level as selected by jumpers at PCB pads 8, 9, and 10. Refer also to Addressing Multiple Mainframes.
21 & 45 thru 50	5 thru 11	Instrument mainframe addresses one through seven.	Seven lines (through connections) used to address up to seven succeeding voltage sources.
18	13	Control word strobe	Single line which accepts a 500 ns, or longer, pulse to load the control word portion of the program data into the 4200-09 assembly. (Refer also to Dual-Strobe Operation) Either logic level may be used as selected by jumpers on PCB pads, 5, 6 and 7.
36	14	Data word strobe	Single line which accepts a 500 ns, or longer, pulse to load the data word portion of the program data into the 4200-09 assembly. (Refer also to Dual-Strobe Operation) Either logic level may be used as selected by jumpers on PCB pads 22, 23 and 24.
9	12	Poll status	Single line used to poll status (Vcc failure and current limit mode). A logic 0 causes the generation of Vcc and current limit status of their respective outputs.
29	22	Polled current limit flag	Single line which generates a logic 0 when the polled 4200 is in the current limit mode.
28	21	Polled power-off flag	Single line which generates a logic 0 when the Vcc supply of the polled 4200 fails (power off).
	23	Abnormal status	Single line which generates a logic 0 whenever the 4200 goes to the current limit mode or the Vcc supply fails (power off). This status lines does not need to be polled.
30	27	Vcc	Single line which provides Vcc to the status logic on the 4200-09. (This is necessary in order to obtain polled power-off status when power is off.) Current requirement is two milliamperes per power source.
16	25	Ready Flag	Single line which provides a logic 0 when any 4200-09 is not ready to receive a strobe signal. This signal is present while the 4200 is changing output voltage as result of a previous strobe signal.

Table 6-2. INPUT/OUTPUT SIGNALS, BINARY PROGRAM SOURCE (Sheet 1 of 2)

PIN NUMBER		SIGNAL NAME	DESCRIPTION
50-PIN CONN.	56-PIN CONN.		
42, 19, 44, 43, 24, 25, 8, 38, 10, 11, 40, 39, 14 & 12		Voltage output magnitude	Fourteen lines used to program the output voltage with a binary word. The least significant bit (pins 12 and B) is 2^0; the most significant bit (pins 42 and P) is 2^{13}.
13	32	Strobe control	Single line used to steer the control strobe signal to transfer either the control word portion of the program data or the data portion of the program data. (Refer also to Single Strobe Operation) Either logic level may be used to strobe either portion of the program data, as selected by jumpers on PCB pads 2, 3 and 4.
26	53	Polarity (Sign)	Single line to program output polarity. Either polarity can be programmed by either logic level as selected by jumpers on PCB pads W, X and Y.
1	27	Output magnitude range	Single line to program output magnitude range on those voltage sources requiring range selection. (Logic 1 = high range, Logic 0 = low range)
31	55	External reference	Single line to program external reference mode on those voltage sources equipped with the external reference option. (Logic 1 = ext reference, Logic 0 = int reference.)
2	28	Current limit range	Single line to program range of current output limiting on those voltage sources equipped current limit selection. (Logic 1 = 1 amp range, Logic 0 = 100 mA range.)
37, 35, 5 & 3	4, 3, 2 & 1	Current limit magnitude	Four lines to select the current limit value, expressed as a percentage of the programmed range. Up to 120% can be programmed. Any attempt to program 0% results in 10%.
17	45	Standby/operate (address zero)	Single line used to select the standby or operate mode of the voltage source. Either mode can be programmed by either logic level as selected by jumpers at PCB pads 18 and 19.
23, 22, 34	46 thru 52	Standby/operate (addresses one through seven)	Seven lines (through connections) used at select the standby or operate mode of up to seven succeeding voltage sources.
20	12	Instrument mainframe (address zero)	Single line used to address the voltage source in order to perform any programming function. The addressing signal must be present in order for any strobe signal to be recognized by the 4200-09 logic. Addressing may be by either logic level as selected by jumpers at PCB pads 8, 9 and 10. Refer also to Addressing Multiple Mainframes.

Table 6-2. INPUT/OUTPUT SIGNALS, BINARY PROGRAM SOURCE (Sheet 2 of 2)

PIN NUMBER		SIGNAL NAME	DESCRIPTION
50 - PIN CONN.	56-PIN CONN.		
21 & 45 thru 50	5 thru 11	Instrument mainframe addresses one thru seven	Seven lines (through connections) used to address up to seven succeeding voltage sources.
18	13	Control Word Strobe	Single line which accepts a 500 ns, or longer, pulse to load the control word portion of the program data into the 4200-09 assembly. In a single-strobe system, also loads the data word portion of the program data when the Strobe Control level is in the opposite state. (Refer also to Single-Strobe and Dual-Strobe operation) Either logic level may be used, as selected by jumpers at PCB pads 5, 6 and 7.
36	14	Data word strobe	Single line which accepts a 500ns, or longer, pulse to initiate the transfer of the data word portion of the program data. (Refer also to Multi-Strobe Operation) Either logic level may be used as selected by jumpers on PCB pads 22, 23 and 24.
9	12	Poll status	Single line used to poll status (Vcc failure and current limit mode). A logic 0 causes the generation of Vcc and current limit status at their respective outputs.
29	22	Polled current limit flag	Single line which generates a logic 0 when the polled 4200 is in the current limit mode.
28	21	Polled power-off flag	Single line which generates a logic 0 when the Vcc supply of the polled 4200 fails (power off).
27	23	Abnormal status	Single line which generates a logic 0 whenever the 4200 goes to the current limit mode or the Vcc supply fails (power off). This status line does not need to be polled.
30	24	Vcc	Single line which provides Vcc to the status logic on the 4200-09. (This is necessary in order to obtain polled power-off status when power is off.)
16	25	Ready flag	Single line which provides a logic 0 when the 4200-09 is not ready to receive any strobe signals. This signal is present while the 4200 is changing output voltage as a result of a previous strobe signal.

TABLE 6-3. 4200-09 JUMPER REQUIREMENTS (Sheet 1 of 2)

DESIRED CONDITION	REFERENCE TEST (paragraph number)	MAKE JUMPER CONNECTIONS
Sixteen-bit data word; eight-bit control word	6-9	T to U
Eighteen-bit data word; six-bit control word	6-9	T to S
BCD data word - positive true	6-15	W to V, J to L, M to K
BCD data word - negative true	6-15	W to V, J to K, M to L
Binary data word - positive true	6-15	W to X, J to L, M to K
Binary data word - negative true	6-15	W to Y, J to K, M to L
Control word - positive true	6-19	N to R
Control word - negative true	6-19	N to P
Polarity bit in 18-bit BCD data word; or in eight-bit control word (see pads S, T and U)	6-21	14 to 15, 16 to 17, H to F, E to B, D to C
Polarity bit in 16-bit binary data word as last bit (see Figure 6-5)	6-21	17 to 14, H to G, A to B
Standby/operate bit synchronous and positive-true (standby = true)	6-23	19 to 16, N to R
Standby/operate bits synchronous and negative-true (operate = true)	6-23	20 to 16, N to P
Standby/operate bit asynchronous and positive-true (standby = true)	6-23	19 to 20
Standby/operate bit asynchronous and negative-true (operate = true)	6-23	18 to 20
Single-strobe operation (binary data only) with true (pos.) strobe control to load control word	6-26	2 to 4, 11 to 12
Single-strobe operation (binary data only) with true (pos.) strobe control to load data word	6-26	3 to 4, 11 to 12
Dual-strobe operation (BCD or binary data)	6-26	1 to 4, 11 to 13
Control word strobe - positive	6-30	5 to 7

Table 6-3. 4200-09 JUMPER REQUIREMENTS (Sheet 2 of 2)

DESIRED CONDITION	REFERENCE TEST (paragraph number)	MAKE JUMPER CONNECTIONS
Control word strobe - negative	6-30	22 to 23
Data word strobe - positive	6-30	23 to 24
Data word strobe - negative	6-30	8 to 10
Mainframe address line enable-positive	6-37	8 to 10
Mainframe address line enable-negative	6-37	9 to 10
Data transferred by control word strobe	6-39	$\overline{G}$ to $\overline{H}$, $\overline{D}$ to $\overline{E}$
Data transferred by data word strobe	6-39	$\overline{E}$ to $\overline{F}$, $\overline{H}$ to $\overline{J}$
Data transferred by data word strobe or control word strobe	6-39	$\overline{E}$ to $\overline{F}$, $\overline{G}$ to $\overline{H}$
Complement last bit of data word	6-48	$\overline{A}$ to $\overline{B}$
Not-complement last bit of data word	6-48	$\overline{A}$ to $\overline{B}$

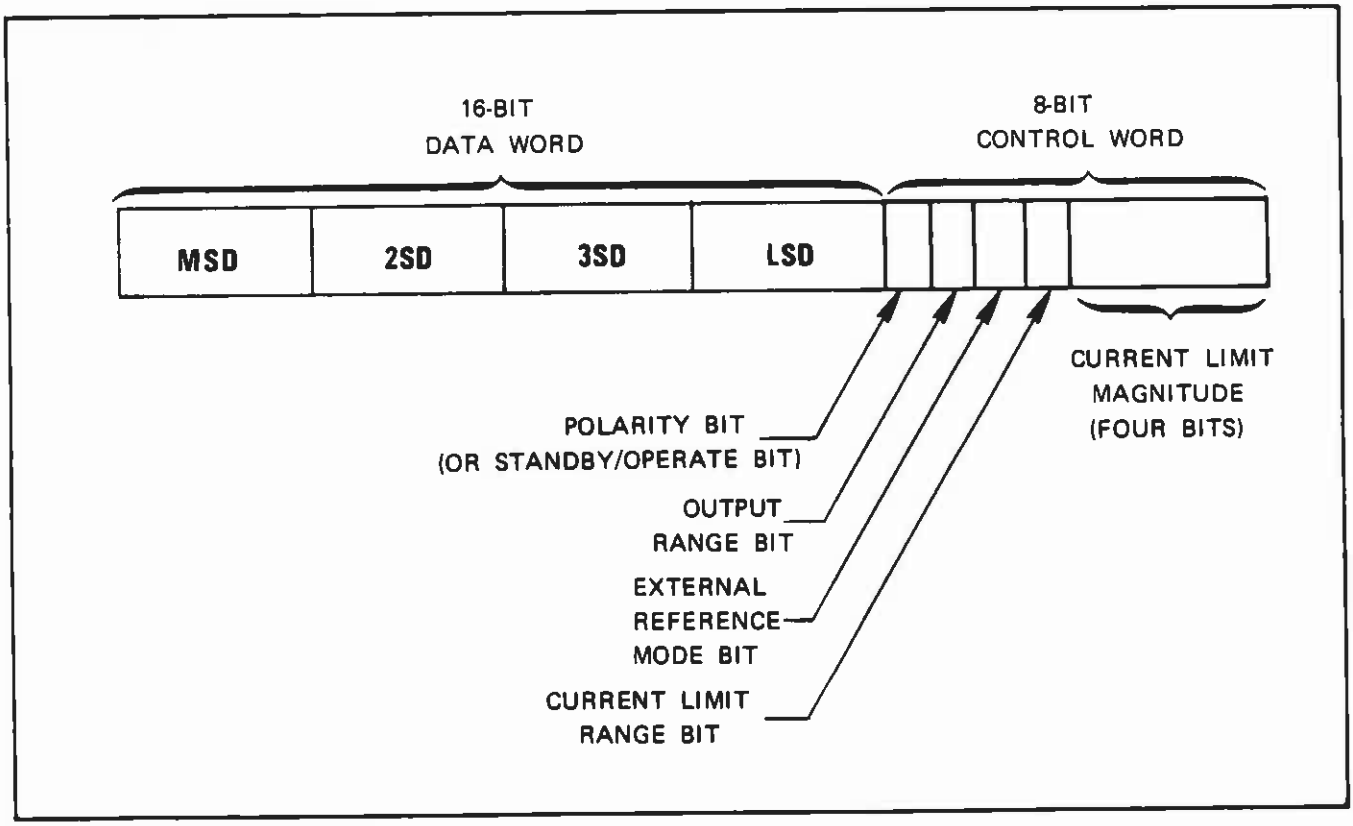


Figure 6-3. BCD PROGRAM DATA, TYPICAL 16-BIT DATA WORD, 8-BIT CONTROL WORD

6-12. When the power source to be programmed requires only output magnitude, polarity and range data, an 18-bit data word, as illustrated in Figure 6-4, can be used without the control word. The control word is necessary when it is required to program the external reference function and current limiting. To obtain an 18-bit data word, jumper pad T to pad S.

6-13. Binary-Type Voltage Sources

6-14. As shown in Figure 6-5, both 16-bit and 18-bit data words may be used with binary-type voltage sources. As described for the BCD-type voltage sources, either the 16-bit or 18-bit data word may be selected, depending upon the system and voltage source requirements. That is, if the voltage source is not equipped with external reference and current limit magnitude selection, the six-bit control word is of no value and an 18-bit data word provides sufficient program data.

6-15. DATA WORD POLARITY

6-16. BCD –Type Voltage Sources

6-17. The 16 or 18 bits which make up the data word portion of the program data may be either positive-true or negative-true as determined by jumpering pads J, K, L, M, V and W. For either logic polarity of BCD data, pad V is jumpered to pad W. For positive-true logic, jumper pad J to pad L and pad M to pad K. For negative-true logic, jumper pad J to pad K and pad L to pad M. (Refer also to Table 6-3.)

NOTE!

Positive-true logic employs +5 volts for a logic 1 and zero volts for a logic 0.

6-18. Binary-Type Voltage Sources

6-19. The logic polarity (i.e. positive-true or negative-true) of the binary data word is determined in much the same manner as that described for the BCD data word. However, pad W is jumpered to pads X or Y (Refer to Table 6-3) instead of pad V.

6-20. CONTROL WORD POLARITY

6-21. The logic polarity for the control word, in either BCD or binary voltage sources, is determined by jumpers at pads N, P and R. If the control word uses positive-true logic, jumper pad N to pad R. If the control word uses negative-true logic, jumper pad N to pad P.

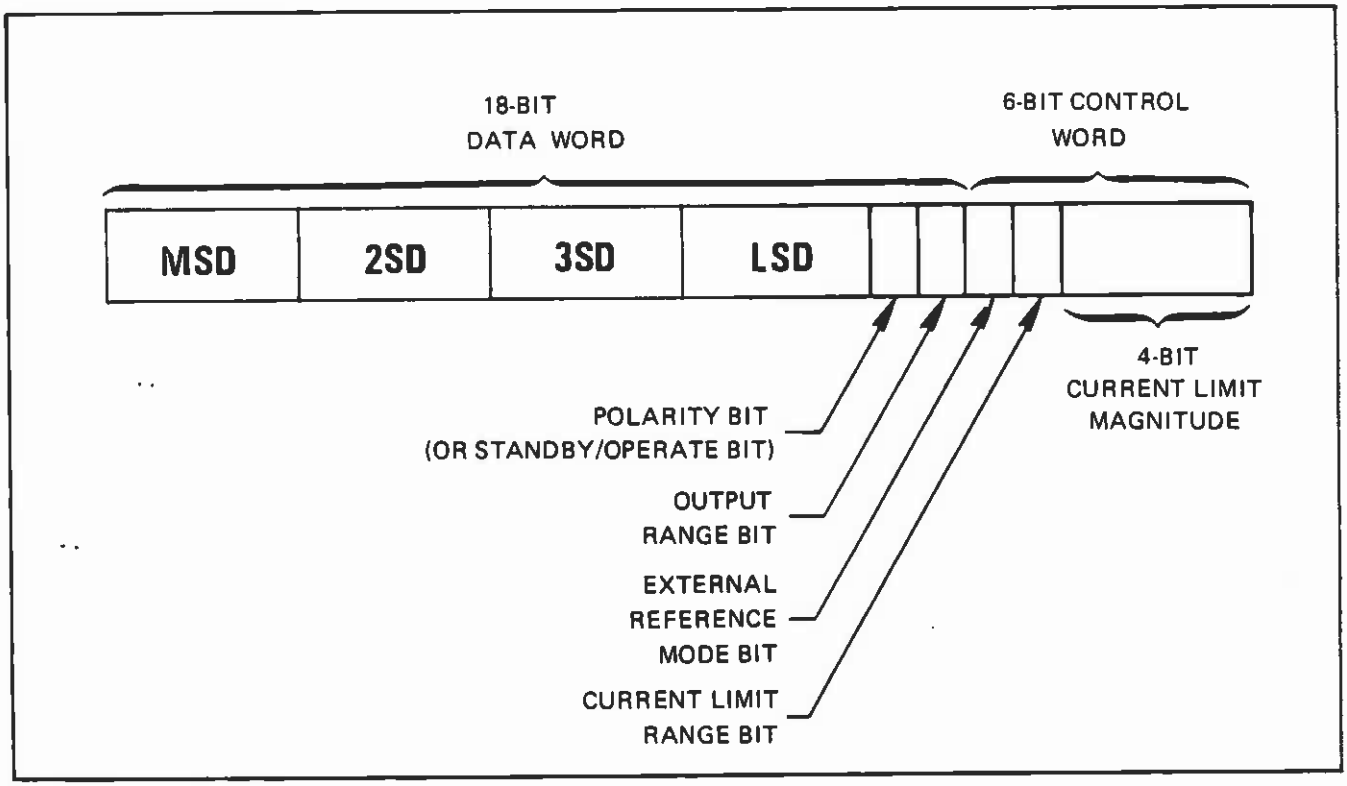


Figure 6-4. BCD PROGRAM DATA, TYPICAL 18-BIT DATA WORD, 6-BIT CONTROL WORD

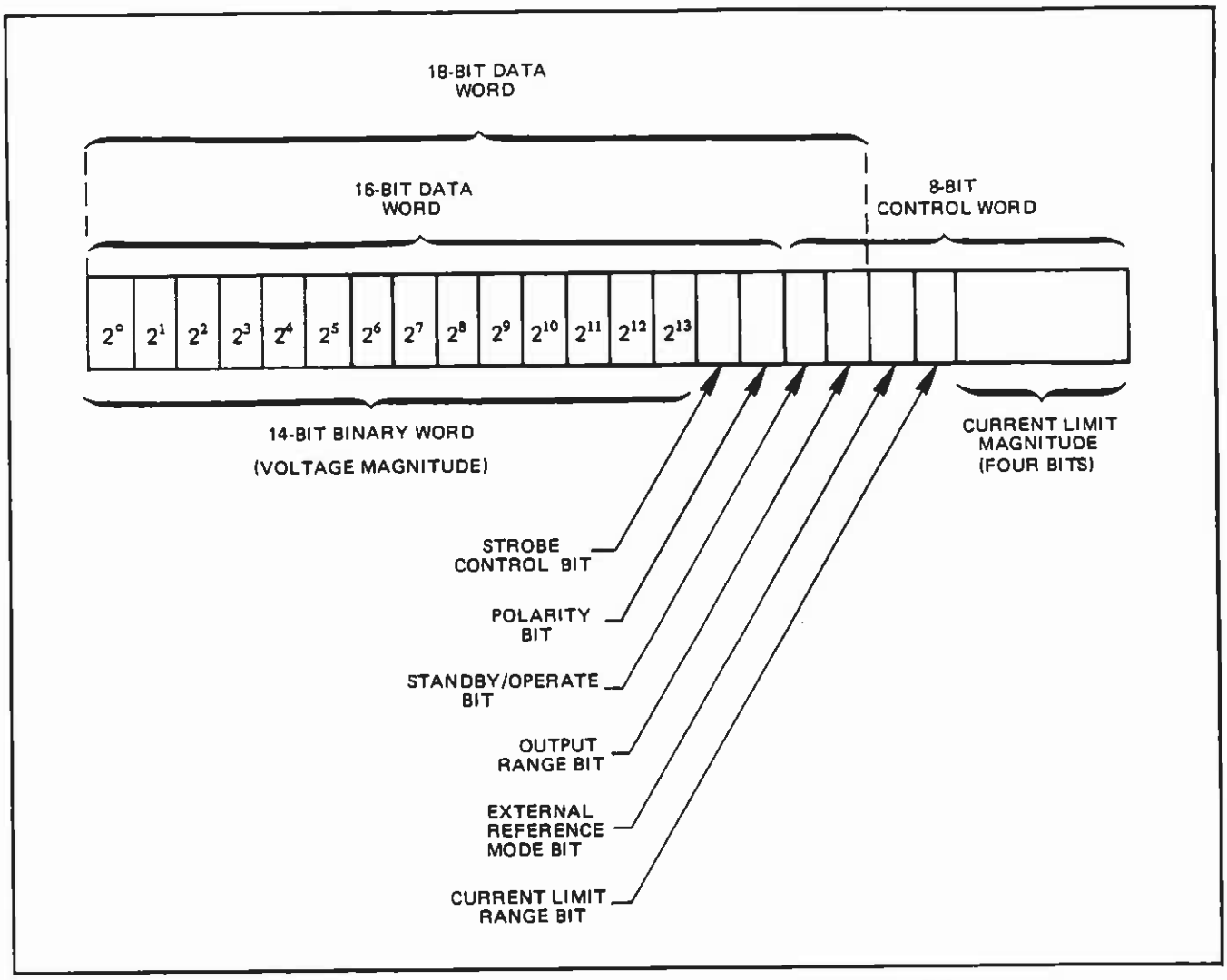


Figure 6-5. BINARY PROGRAM DATA, TYPICAL 16-BIT AND 18-BIT DATA WORDS

6-22. OUTPUT VOLTAGE POLARITY BIT LOCATION

6-23. Selection of the voltage source output polarity (positive or negative) is made by means of a polarity bit which may be placed in an 18-bit BCD data word, an eight-bit control word, or a 16-bit binary data word. The placement of the polarity bit in the 18-bit BCD data word or the eight-bit control word (BCD or binary programming) is determined by the Data Word/Control Word Length assignment; i.e. pads S, T and U. Refer to Table 6-3 for pad jumpering details to place the polarity bit in the 18-bit BCD data word or the 16-bit binary data word.

6-24. STANDBY/OPERATE – SYNCHRONOUS OR ASYNCHRONOUS

6-25. Each of the 4200 series power sources can be commanded to the operate and standby modes by means of a unique standby/operate line from the program source. The standby/operate command can be jumpered so that it is synchronous with the transfer of the data word and/or control word. The standby/operate command can also be jumpered so that it is asynchronous. That is, the particular power source goes to the standby or operate mode immediately upon command by the program source, without waiting for a program data transfer function (strobe pulse).

6-26. To make the standby/operate command synchronous, a standby/operate bit crosses the guard as the first bit of an eight-bit control word, as shown in Figure 6-5. To make the standby/operate command synchronous, jumper pad 19 to pad 16 and pad N to pad R (for standby true) or pad 20 to pad 16 and pad N to pad P (for operate true). To make the standby/operate command asynchronous (independent of program data transfers), jumper pad 19 to pad 20 for standby-true, or pad 18 to pad 20 for operate true.

6-27. SINGLE/DUAL – STROBE OPERATION

6-28. The 4200-09 can program output voltages in both single-strobe and dual-strobe modes. BCD-type voltage sources are usually operated in the dual-strobe mode, while binary-type voltage sources may be operated in either mode. The single-strobe mode refers to the use of a single strobe line (but two strobe pulses) to load both the data word and the control word from the program source into the 4200-09 assembly. Which of the two words (data or control) loaded depends upon the logic level applied to the strobe control line. In single-strobe operation, the binary data word is into the 4200-09 storage resistors (in preparation for transfer to the voltage source) by placing the proper logic level on the strobe control line (Refer to Table 6-3 for strobe control line logic levels) and placing a strobe pulse on the control word strobe line (pin 18). The control word is loaded into storage registers by placing the opposite logic level on the strobe control line and placing a second strobe pulse on the control word strobe line. In this manner, a single strobe line is used to load both the data and control words into storage registers by changing the logic level on the strobe control line. This system is usually used with binary program and voltage sources.

6-29. The dual-strobe mode refers to the use of two separate strobe pulses on two separate lines to load the data word and control word from the program source into storage registers in preparation for transfer to the voltage source. This mode is usually used when the data word is BCD. The data word strobe line (pin 36) is used to load the 16-bit or 18-bit data word, while the control word strobe line is used to load the control word.

6-30. To operate the 4200-09 in the single-strobe mode, jumper pad 2 to pad 4 and pad 11 to pad 12, if a positive strobe control signal level is used to load the control word; or jumper pad 3 to pad 4, and pad 11 to pad 12, if a positive strobe control signal level is used to load the data word. To operate in the dual-strobe mode, jumper pad 1 to pad 4, and pad 11 to pad 13.

6-31. CONTROL/DATA WORD STROBE SIGNALS

6-32. Control Word Strobe, Single-Strobe Mode

6-33. The control word strobe signal is a 500 nanosecond, or longer, pulse which is issued by the program source after the control word and/or data word has been applied to the parallel data inputs of the 4200-09 assembly. In the single-strobe mode, the control word strobe is used to load the control word from the program source into the 4200-09 storage registers when the strobe control line is at the appropriate logic level (determined by pads 2, 3 and 4). When the strobe control line is at the other logic level, the control word strobe loads the data word into the registers. If the control word strobe is a positive-going (zero to +5Vdc) pulse, jumper pad 5 to pad 7. If the control word strobe is a negative-going (+5Vdc to zero) pulse, jumper pad 6 to pad 7.

6-34. Control Word Strobe, Dual-Strobe Mode

6-35. As in the single-strobe mode, the control word strobe is a 500 nanosecond, or longer, pulse which is issued by the program source, the program data is applied to the parallel inputs of the 4200-09 assembly. In the single-strobe mode, the control word strobe load the control word only, into the storage registers. (The data word is transferred by a data word strobe signal.) If the control word strobe is a positive-going pulse, jumper pad 5 to pad 7. If the control word strobe is a negative-going pulse, jumper pad 6 to pad 7.

6-36. Data Word Strobe

6-37. The data word strobe signal is used in the dual-strobe mode to load the data word, applied to the parallel data word inputs of the 4200-09 assembly, into the storage registers. The data word strobe is a 500 nanosecond, or longer, pulse which is issued by the program source after the data word has been applied to the parallel inputs of the 4200-09 assembly. If the data word strobe is a positive-going (zero to +5Vdc) pulse, jumper pad 8 to pad 10. If the data word strobe is a negative-going (+5Vdc to zero) pulse, jumper pad 9 to pad 10.

6-38. MAINFRAME ADDRESS SIGNAL LEVEL

6-39. In order for the 4200-09 to receive and program data, it must be addressed at the time of the strobe signal (s). The mainframe address signal is a +5 volt or ground level signal applied to the address line number zero of the 4200-09 to be addressed (Refer also to paragraph 6-53). If a +5 volt signal is to be used for mainframe addressing, jumper pad 8 to pad 10. If a ground level is to be used, jumper pad 9 to pad 10.

6-40. PROGRAM DATA TRANSFER

6-41. General

6-42. The generation of the control word strobe and data word strobe signals by the program source loads the

program data into storage registers within the 4200-09 assembly. From the storage registers, the program data (control word and data word) is transferred in serial fashion (bit-by-bit) across the guard shield to the digital-to-analog converter within the voltage source. The serial transfer of program data is initiated after a short delay by the trailing edge of the control word strobe, or the data word strobe, or both, as determined by pads D, E, F, G, H and J.

NOTE!

The power source output voltage does not change to the newly programmed value until data transfer is completed.

6-43. Data Transfer By Control Word Strobe

6-44. To initiate the transfer of the program data (the control word and the data word) from the storage registers to the digital-to-analog converter within the power source by means of the control word strobe, jumper pad G to pad H. To prevent data transfer at the occurance of a data word strobe, jumper pad D to E.

6-45. Data Transfer By Data Word

6-46. To initiate transfer of the program data by means of the data word strobe, jumper pad E to pad F. To prevent data transfer at the occurance of a control word strobe, jumper pad H to pad J.

6-47. Data Transfer By Control Word Or Data Word Strobe

6-48. To initiate transfer of the program data by means of either the control word strobe or the control word strobe, jumper pad E to pad F, and pad G to pad H.

6-49. COMPLEMENTING BINARY PROGRAM DATA

6-50. Binary data words supplied by the program source which represent negative voltage outputs are two's complemented, and must be re-complemented in order to obtain the required output polarity at the power source. When jumpering is performed to receive binary data from the program source (pads J, K, L, M, W, X, Y), complementing to accomodate data word polarity is automatically performed. However, additional jumpering is required in order to properly handle the polarity indication for the binary data word (power source output magnitude). The polarity (positive or negative) of the power source output may be indicated by means of:

a. the last (16th) bit of the binary data word.

b. a polarity bit as part of the control word.

6-51. If the polarity is indicated in the last bit of the binary data word, following the 14-bit magnitude data and strobe control bit (as shown in Figure 6-5), it must not be complemented along with the data word. To prevent this last bit of the data word from being complemented, jumper pad A to pad B. If the polarity is indicated by a bit within the control word, the entire data word should be complemented (when necessary) by jumpering pad A to pad C. (This is only necessary when transferring all 16 bits of binary data to a 4275A.)

6-52. ADDRESSING MULTIPLE MAINFRAMES

6-53. Up to eight separately addressable 4200 series power sources may be connected to a single program source when each are equipped with the 4200-09. Figure 6-2 shows the method of multiple power source connections using factory-manufactured cable assemblies. The power source electrically closest to the program source is numbered zero, and the succeeding power sources are numbered in ascending order, up to seven. The mainframe address signals, which are +5 volts or ground levels, are supplied to the power sources for the duration of the programming sequence. All mainframe address signals must be applied to the mainframe address inputs of the first power source (number zero). That is, the program source is only connected directly to the first power source, and connection to subsequent power sources is handled by means of through connections on the 4200-09 assembly.

6-54. The mainframe address signals may be either +5 volts or ground as determined by jumpers 8, 9 and 10. All signals are applied to the mainframe address lines of the first 4200-09 mainframe, address line number zero enables the first 4200-09 mainframe, to accept program data and strobe signals. As shown in Figure 6-6, mainframe address line number one is fed through the first 4200-09 to exit at its zero address output for application to the next power source. The mainframe address lines are shifted by one position each time they pass through a 4200-09. In this manner, each power source is directly addressed at its zero address input although the program source selects the

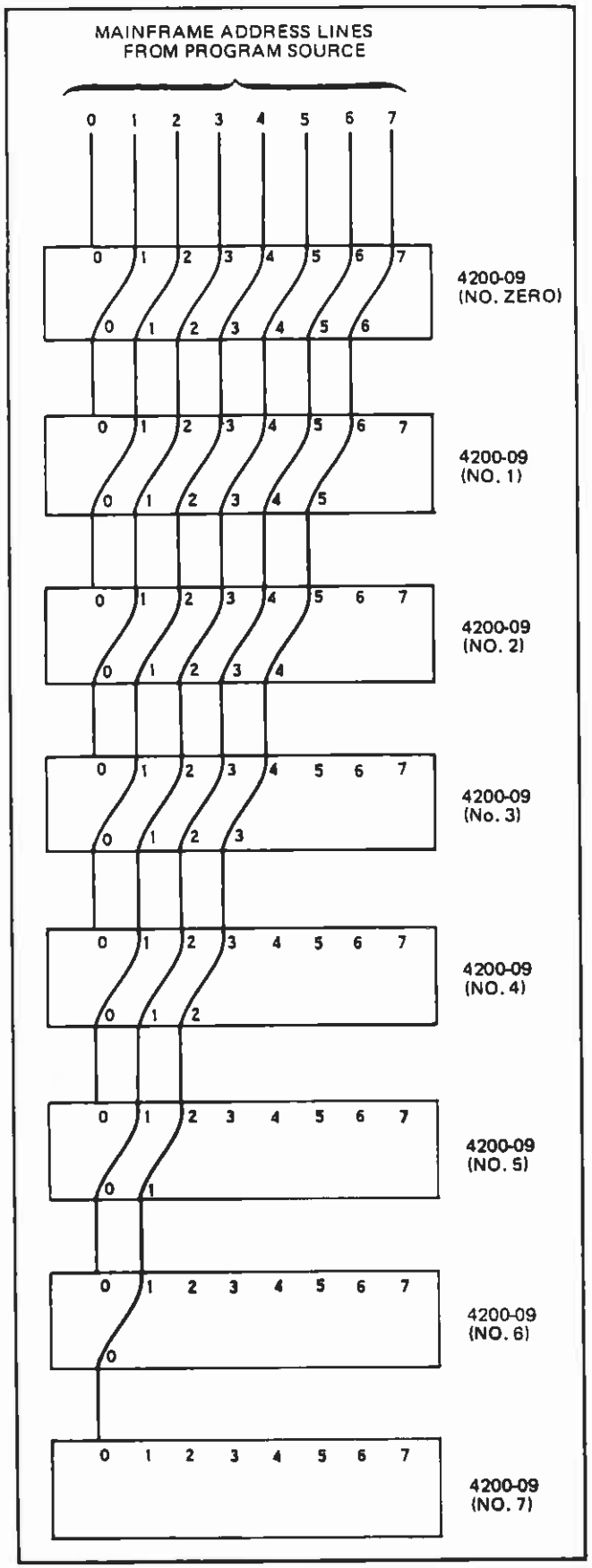


Figure 6-6. MULTIPLE MAINFRAME ADDRESSING

different 4200-09 assemblies at the mainframe address lines on the first 4200-09 (number zero). Several power sources may be addressed at one time, and each will receive the program data. Table 6-4 lists the pin numbers of the 50-pin connector (located on the rear panel of the first power source) on which the different 4200-09 assemblies are addressed by the program source.

Table 6-4. MAINFRAME ADDRESSES – PIN ASSIGNMENTS

POWER SOURCE MAINFRAME ADDRESS	PIN NUMBER (50-pin connector on power source no. zero)
0	20
1	50
2	49
3	48
4	47
5	46
6	45
7	21

NOTE!

In single-strobe binary operation, the mainframe address need only be present when transferring the control word. When transferring the data word, the power source which last received a control word is automatically addressed, unless another mainframe address is specified.

6-55. CHECKING STATUS

6-56. Introduction

6-57. The 4200-09 provides four separate status indicators (flags) which are bussed with the status flags from all other power sources in the system, back to the program source. The four status flags are provided on four separate lines and include the following:

a. Abnormal status (power-off or current limit) flag.

b. Polled current limit flag.

c. Polled power-off flag.

d. Not ready flag.

NOTE!

All flag lines are wire-ored to an open collector bus. Pull-up resistors are required in the program source interface to enable the flags to reach +5 volts.

6-58. Status checking the 4200-09 is typically handled by the program source in such a manner that the abnormal status flag is allowed to interrupt. As a result of the interrupt, the program source may poll each 4200-09 in the system while monitoring the polled current limit flag bus and polled power-off flag bus for a flag indication. The not ready flag is not polled, and when present, indicates that one or more power sources is still acting on program commands, and is not yet ready to receive further commands.

6-59. Polled Current Limit Flag

6-60. As shown in Figure 6-7, the polled current limit flag bus appears on pin 29 (on the 50-pin connector) of any 4200-09 in the system. The flag is polled by placing a ground level on the poll status input (pin 9) of the particular 4200-09 being polled. If the current limit flag bus responds with +5 volts, the current limit condition for the polled power source does not exist. However, if the current limit flag bus responds with a ground level, the current limit condition does exist, and an overloaded power source is indicated.

6-61. As illustrated in Figure 6-7, the poll status inputs to several 4200-09 in a system are not normally bussed together, but may be individually polled by the program source. A typical method of polling the status is to jumper the mainframe address line (number zero) from pin number 20 to the poll status input at pin number 9. In this manner, status is available at the current limit flag bus (and the power-off flag bus) whenever the particular 4200-09 is addressed.

6-62. Polled Power-Off Flag

6-63. Polling the power-off flag is identical to that described for the current limit flag except some external source of +5 volts must be applied to pin number 30. The +5 volt source is required in order to obtain the power-off status indication when the power to the polled unit has actually failed. The power-off status indication is a ground level on the power-off flag bus.

6-64. INPUT LOADING

6-65. Each input to each 4200-09 used in the system represents a single TTL input load. With a full complement

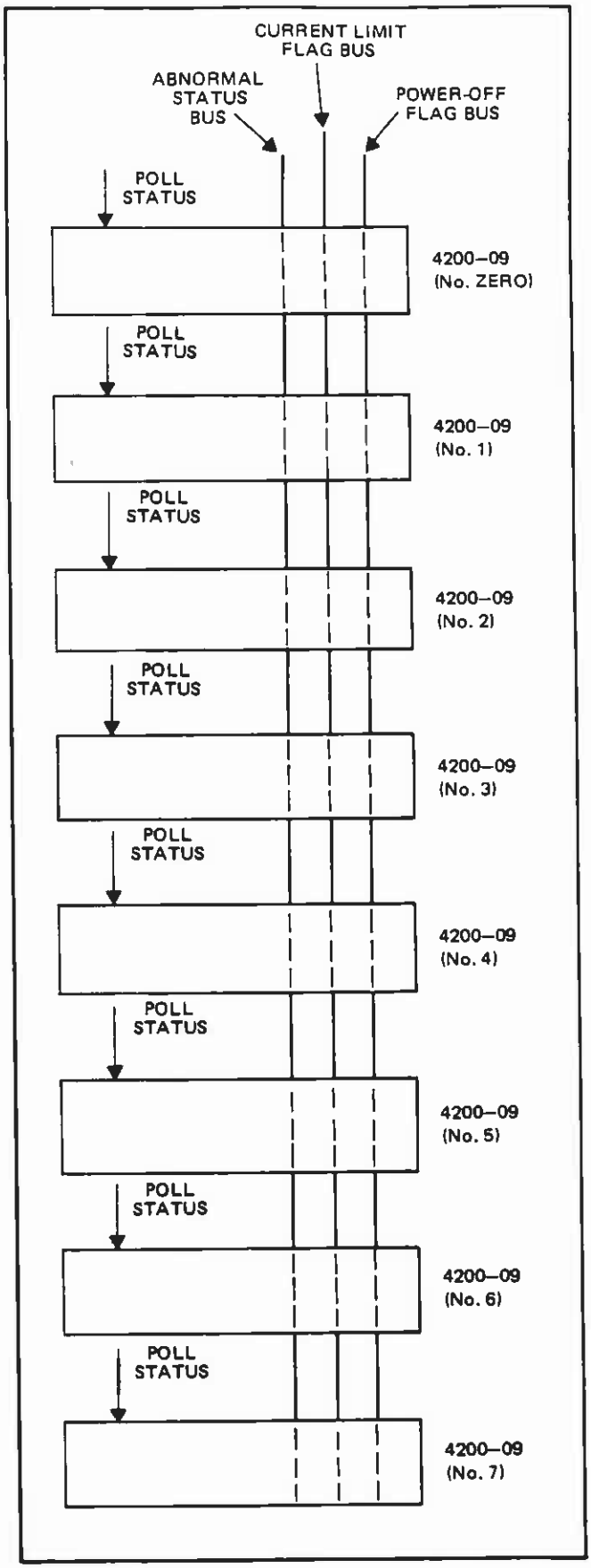


Figure 6-7. STATUS BUSSES LAYOUT

of eight power sources in the system, the power requirements for each input of the first power source are increased by a factor of eight, except for the Mainframe Address and the Standby/Operate which are always single loads.

6-66. THEORY OF OPERATION

6-67. General Description

6-68. The 4200-09 can be configured (by means of jumpers) to accomodate a large number of program environments. Consequently, theory discussions are somewhat generalized, since all configurations cannot be described. In any application, the main function of the 4200-09 is to receive output magnitude and control data from a program source in parallel form, transfer the data across the power source guard shield, and present the data to the power source digital-to-analog converter. Figure 6-8 shows a simplified block diagram of the 4200-09 and how the data and control words, generated by the program source in parallel form, are applied to shift registers which perform a parallel-to-serial conversion.

6-69. Upon the receipt of a data word strobe or control word strobe, the control logic generates a load command to one or both shift registers. The data word and control word supplied by the program source, and present at the shift register inputs, is loaded into the shift registers. When the shift registers are loaded with the program data, the control logic starts a 10 MHz clock and issues a hold command to the power source.

6-70. The output pulses from the clock are fed to the shift registers to move the program data out of the registers, bit-by-bit, to the coupling transformers at the guard shield. The data word is shifted out of its respective storage register via two's complementing logic which is enabled when the program source indicates that the data word is a negative binary number. This action is necessary since the 4200 binary power source requires positive binary numbers (in conjunction with a positive or negative polarity indicator). The control word undergoes no complementing at any time.

6-71. While the program data is being shifted across the guard shield by the clock pulses, the clock pulses are also being fed across the guard shield, and the hold one-shot is triggered as a result of the hold command issued by the control logic. On the inside of the guard shield, the clock pulses are used to shift the serial program data into shift registers which provide the necessary serial -to-parallel conversion. (The 4200 power sources require parallel program data.) The output of the hold one-shot is present for the duration of the serial data transfer across the guard shield. This action is necessary to inhibit any change in power source output magnitude while the data word is being serially loaded into the shift register.

6-72. The control word portion of the program data is also loaded into a shift register, and is double-buffered to prevent any change in power source output while loading is taking place. The double-buffering is provided by a series of latch circuits which receive a load pulse from a latch timing circuit. The latch timing circuit issues the load pulse to the latch circuits sometime after the last clock pulse when all data has been shifted into the registers. As the load pulse occurs, the latch circuits are loaded with the control word and present it in parallel form to the 4200 power source. (Double-buffering for the data word is not required since the hold signal "freezes" the power source output magnitude until the data word is completely loaded into the shift register.)

6-73. The shifting and loading of the program data is performed by the clock pulses. The start of the clock pulses is a function of the control logic. The stopping of the clock is also performed by the control logic, but after the generation of 16 pulses. When the clock is stopped, all shifting action ceases; and after the fold signal disappears and the load pulse to the latch occurs, all program data is presented to the digital-to-analog converter within the 4200 power source. At this time, the power source assumes its newly programmed output.

6-74. BLOCK DIAGRAM ANALYSIS

6-75. Input Sequence

6-76. Figure 6-9 shows that the parallel program data, supplied by the program source, is applied to a pair of shift registers as well as to the succeeding 4200 power source (s) in the system. The data is loaded into the register (s) when the appropriate strobe signal is received from the program source.

6-77. In a device configured for single-strobe operation, the control word strobe signal (in conjunction with the strobe control line) is used to load both the data word and control word into their respective registers. The strobe signal gating accepts the control word strobe from the program source, and depending upon the state (+5 volts or ground) of the strobe control line, directs the strobe signal to either the control word one-shot or the data word one-

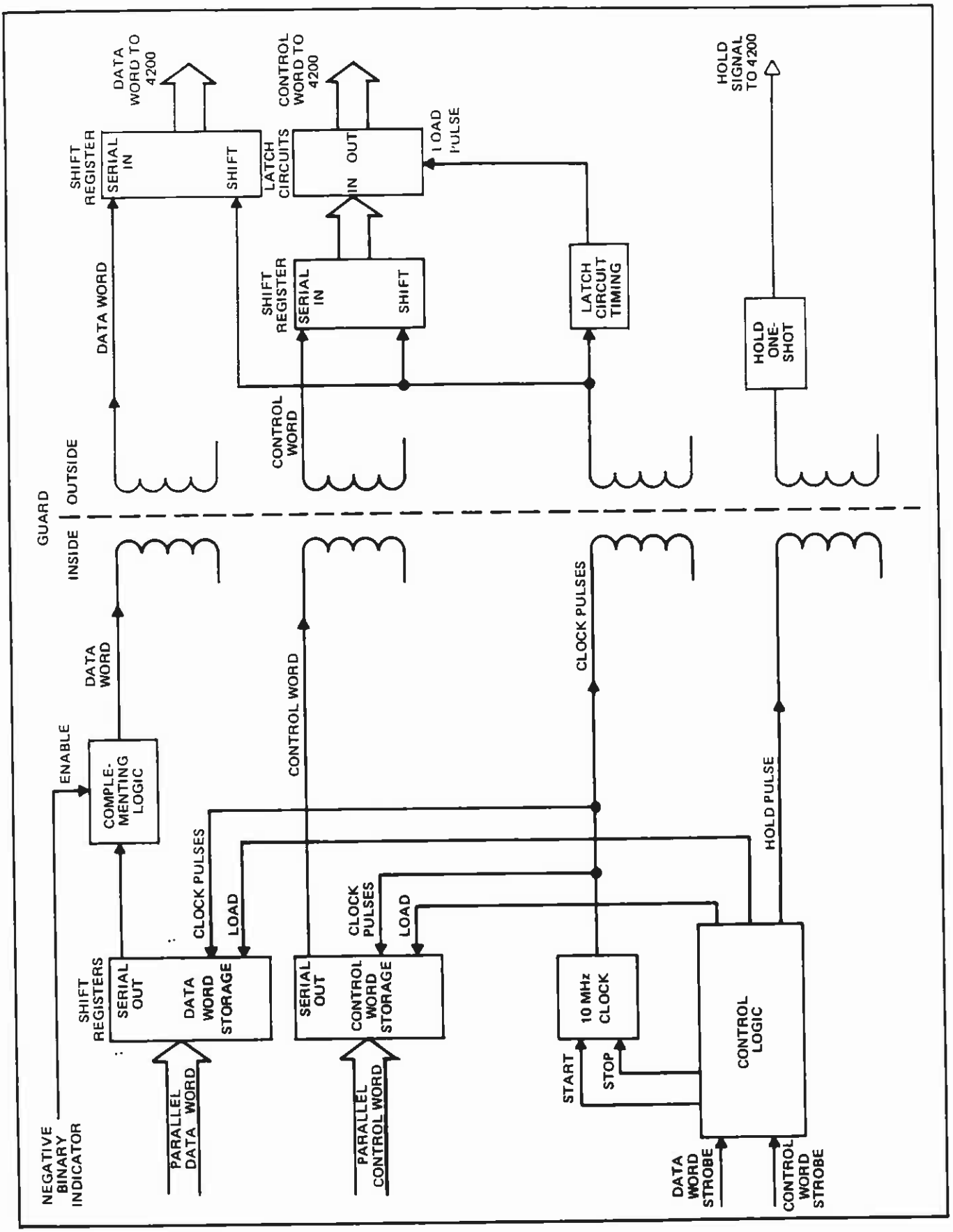


Figure 6-8. 4200-09, SIMPLIFIED BLOCK DIAGRAM

shot. If the strobe control line directs the control strobe pulse to the control word one-shot, a pulse is generated and fed to the parallel-load input of the control word shift register. The pulse causes the shift register to load the parallel control word supplied by the program source. If the strobe control line directs the control strobe pulse to the data word one-shot, a pulse is fed to the parallel-load input of the data word shift register.

NOTE!

In order for the control word strobe (or the data word strobe) to trigger either of the one-shots, the mainframe address line must be enabled.

6-78. In a device configured for dual-strobe operation, both the control word strobe and data word strobe signals are used to load the program data from the program source. In this configuration, the control word strobe triggers the control word one-shot to load the control word into its shift register, and the data word strobe triggers the data word one-shot to load the data word. (Refer also to Figure 6-10.)

6-79. Data Transfer

6-80. Whenever the control word one-shot or data word one-shot is triggered, the resulting output triggers a first hold one-shot. (Refer also to Figure 6-10.) One output of the hold one-shot produces a hold pulse which is fed across the guard shield (via T2) to trigger a second hold one-shot. The second hold one-shot generates a hold pulse required by the power source to hold the output magnitude at the current value while magnitude data is being re-programmed.

NOTE!

The duration of the hold pulse depends upon the particular power source being used.

6-81. The trailing edge of the other first hold one-shot output (triggered by the strobe signal), sets a data transfer flip-flop. The Q output of the data transfer flip-flop starts a 10 MHz clock, if not already operating (refer to Standby Sequence), and gates the clock pulses to the serial shift inputs of the control word and data word shift registers. (The clock pulses are also gated to the input of a ÷ 16 counter and to the primary winding of T4.) As each clock pulse is received by the shift registers, the previously loaded program data is shifted, serial-by-bit out of the shift registers to the coupling transformers (T3 and T5) at the guard shield. On the inside of the guard shield, the serial data and control words are loaded into a second set of shift registers which are clocked by the pulses at the secondary of T4.

6-82. The clock pulses gated by the data transfer flip-flop are also fed to a 4-bit binary counter which produces a carry pulse at the time of the sixteenth clock pulse. The carry pulse resets the data transfer flip-flop to inhibit the gating of the clock pulses and stop the clock, if the standby mode is not present. (Refer to Standby Sequence.) After the generation and gating of 16 clock pulses the data word has shifted completely around the data word shift register while being transformer-coupled across the guard and into the second shift register for application to the 4200 power source. The control word, since it contains eight bits or less, is actually shifted around the control word register, across the guard and into the second control word register two complete times.

6-83. The control word is double-buffered for application to the 4200 power source. This is necessary since the hold signal, provided during data transfer by the second hold one-shot, does not "freeze" the output range of the 4200 power source, just the output magnitude. To parallel shift the control word from the shift register to a set of latch circuits, the first of the 16 clock pulses triggers a latch timing one-shot which has a pulse width slightly greater the serial data transfer time (16 clock pulses). The trailing edge of the latch timing one-shot output is fed to a pulse generator which provides a load pulse to the latch circuits. At the time of the load pulse, the latch circuits are parallel loaded with the control word for application to the 4200 power source.

6-84. Complementing Binary Data

NOTE!

Complementing magnitude data occurs only in binary-type power sources.

6-85. Binary-type power sources require that negative values of magnitude data be two's complemented since binary program sources usually indicate polarity by means of a single bit and supply two's complemented magnitude data for negative outputs. The binary-type power sources require non-complemented binary data plus a polarity bit. As a result, negative binary magnitude data, consisting of complemented data, must be re-complemented to satisfy the requirements of the power source. When the binary program

source indicates negative sign, U14 is enabled to pass the output of the complementing logic. The complementing logic receives the serial output of the shift registers, complements it, and passes it across the guard via T1.

6-86. Operation of the two's complementing logic is such that the first bit of serial data is present at the output of the shift registers before the ÷ 16 counter and a complement flip-flop receives the first of 16 clock pulses. At this time, the ÷ 16 counter is in its zero state and the complementing flip-flop is still reset (as a result of the carry pulse generated by the ÷ 16 counter at the end of the previous data transfer sequence). With the complement flip-flop reset, the complement logic is not enabled and no inversion of serial data takes place. This condition permits the first bit of binary magnitude data to be transferred without being complemented. However, after the first clock pulse, the complement flip-flop may be allowed to go set (to enable the complement logic), depending upon the state of the J input, which is derived from the serial data. As a result, the complement flip-flop goes set at the time of the first true bit of serial data to enable the inverting logic and complement the remaining bits of serial data. After the 16th bit of data, the complementing flip-flop is reset by the carry output of the ÷ 16 counter.

6-87. Programming the 4200 power source to standby (zero output, but no change in programmed magnitude and range) may be performed in a synchronous or asynchronous manner, depending on jumper configuration. With synchronous standby operation, (not shown in Figure 6-9) the standby bit supplied by the program source becomes part of the control word and is serially shifted across the guard for application to the standby input of the 4200 power source. This mode is referred to as synchronous standby because commanding the 4200 power source to standby or operate is always synchronous with a strobe signal from the program source.

6-88. Asynchronous Standby Operation

6-89. With asynchronous standby operation, the 4200 power source can be commanded to standby or operate at any time by the program source. As shown in Figure 6-9, the standby signal (dc) is gated to the start input of the 10 MHz clock to initiate the generation of clock pulses (if not already being generated during a data transfer sequence of 16 clock pulses). As long as a data transfer sequence is not in progress, the data transfer flip-flop is in its reset state. When the data transfer flip-flop resets the clock pulses are gated through to the primary winding of T6 and are inhibited (by the Q output) from the shift registers and ÷ 16 counter. The secondary winding, located inside the guard, feeds the clock pulses to a half-wave rectifier. The dc output of the rectifiers is fed to the 4200 power source standby/operate input.

6-90. Status Logic

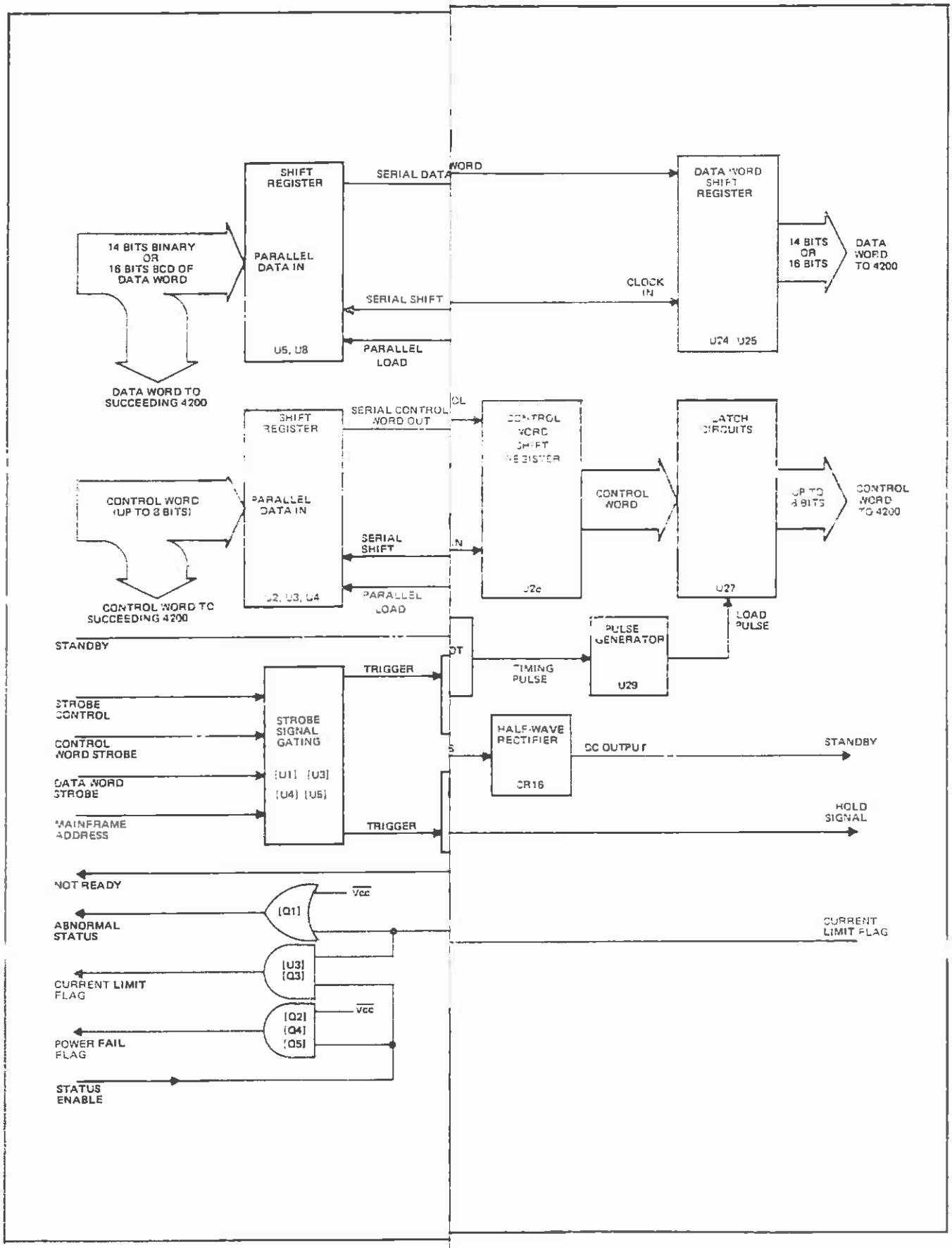
6-91. Two separate status conditions are indicated by the power source equipped with the 4200-09, i.e. current limit mode status and power failure. The current limit status flag is furnished by the 4200 power source whenever an overload condition exists and the current limit function is being used. The power failure indication is provided by the 4200-09.

6-92. The current limit flag is fed from the 4200 power source to enable a current limit oscillator on the 4200-09 (Refer to Figure 6-9). The oscillator output signal is coupled to the outside of the guard via T1, and to the input of a half-wave rectifier. The dc output of the rectifier indicates the current limit condition and appears at the abnormal status output. The current limit flag is also available at the current limit flag output when the program source addresses the unit with a status enable signal.

6-93. The power fail flag results from the failure of the +5 volt supply to the 4200-09, which is indicative of a general power failure within the power source. As in the current limit flag, the power fail flag appears on the abnormal status line, and on the power fail flag output when the unit is addressed with a status enable signal.

6-94. Not Ready Signal

6-95. The 4200-09 generates a not-ready signal to the program source whenever it is not ready to accept program data or strobe signal (s) from the program source. As shown in Figure 6-9 and 6-10, the not ready flag one-shot is triggered by the trailing edge of the first hole one-shot output to generate the not ready flag. The duration of the not ready flag is through the data input sequence to notify the program source that the data is being transferred to the power source and no strobe signal should be generated at this time. The duration of the not ready flag depends upon the type of power source being programmed. The table included on the schematic diagram lists the different component values used and the one-shot periods provided


SHIFT REGISTER
SERIAL DATA WORD
DATA WORD SHIFT REGISTER
14 BITS BINARY OR 16 BITS BCD OF DATA WORD
PARALLEL DATA IN
SERIAL SHIFT
CLOCK IN
14 BITS OR 16 BITS
DATA WORD TO 4200
U5, U8
PARALLEL LOAD
U24 U25
DATA WORD TO SUCCEEDING 4200
SHIFT REGISTER
SERIAL CONTROL WORD OUT
CONTROL WORD SHIFT REGISTER
LATCH CIRCUITS
CONTROL WORD (UP TO 8 BITS)
PARALLEL DATA IN
CONTROL WORD
UP TO 8 BITS
CONTROL WORD TO 4200
SERIAL SHIFT
PARALLEL LOAD
U2c
U27
CONTROL WORD TO SUCCEEDING 4200
LOAD PULSE
STANDBY
PULSE GENERATOR
TRIGGER
TIMING PULSE
U29
STROBE CONTROL
STROBE SIGNAL GATING
CONTROL WORD STROBE
HALF-WAVE RECTIFIER
DC OUTPUT
STANDBY
DATA WORD STROBE
(U1) (U3)
(U4) (U5)
MAINFRAME ADDRESS
TRIGGER
HOLD SIGNAL
CR16
NOT READY
Vcc
(Q1)
ABNORMAL STATUS
CURRENT LIMIT FLAG
(U3) (Q3)
CURRENT LIMIT FLAG
Vcc
(Q2) (Q4) (Q5)
POWER FAIL FLAG
STATUS ENABLE

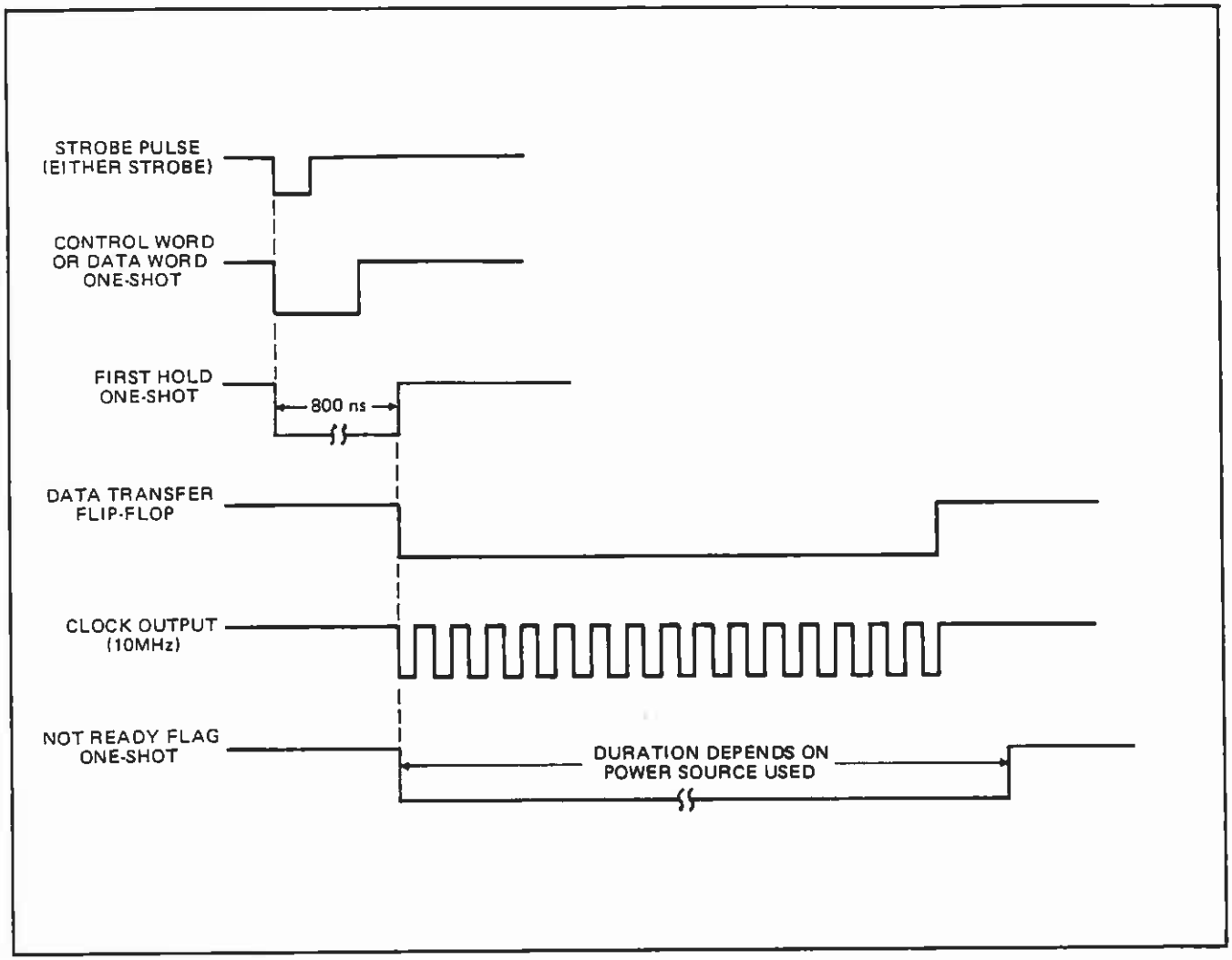


Figure 6-10. INPUT SEQUENCE – TIMING DIAGRAM

for the different 4200 series power sources being programmed.

6-96. MAINTENANCE

6-97. Performance Checks

6-98. Proper operation of the 4200-09 is best verified while in its normal operating environment, i.e. while installed in the power source and connected to the program source. In the system environment, operation of the 4200-09 is typically verified by means of diagnositc routines, or by manually-entered statements at the operator interface, i.e. crt console, teletypewriter, control console, etc. The actual procedure employed to check the 4200-09 depends upon the particular system configuration and is beyond the scope of this manual.

6-99. Calibration

6-100. The 4200-09 requires no periodic or repair calibration.

6-101. Troubleshooting

6-102. The troubleshooting information in the following tables is provided to assist in isolating 4200-09 malfunctions, and is presented in flow chart form. Following the chart from beginning to end will usually identify and localize any malfunction. It is suggested that the preceeding theory of operation be read and the block and schematic diagrams be referenced prior to troubleshooting.

NOTE!

Prior to troubleshooting, place the 4200-09 PCB assembly on an extender card (Fluke part no. 292263).

Table 6-5. TROUBLESHOOTING CHART, INACTIVE PCB ASSEMBLY (Sheet 1 of 2)

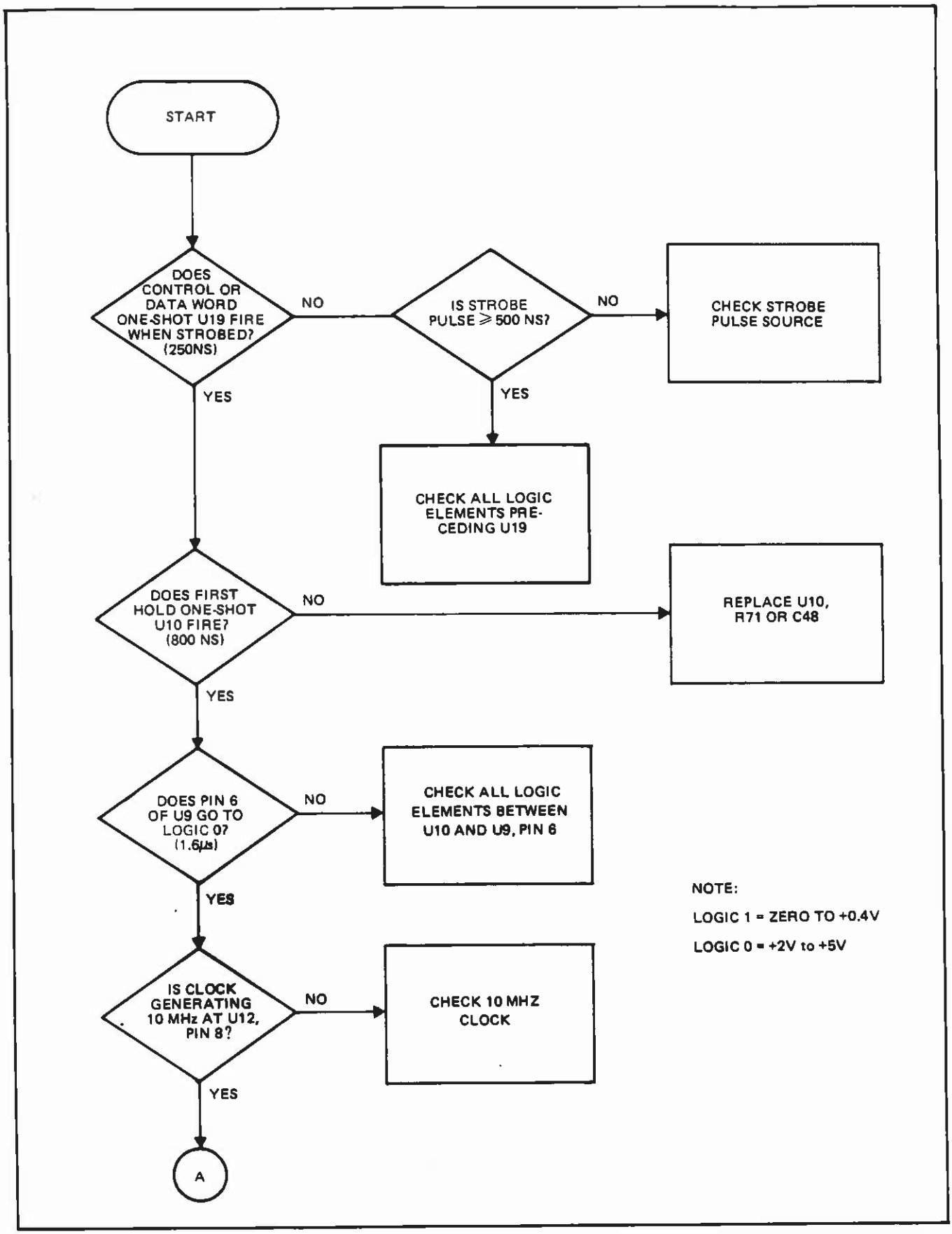


Table 6-5. TROUBLESHOOTING CHART, INACTIVE PCB ASSEMBLY (Sheet 2 of 2)

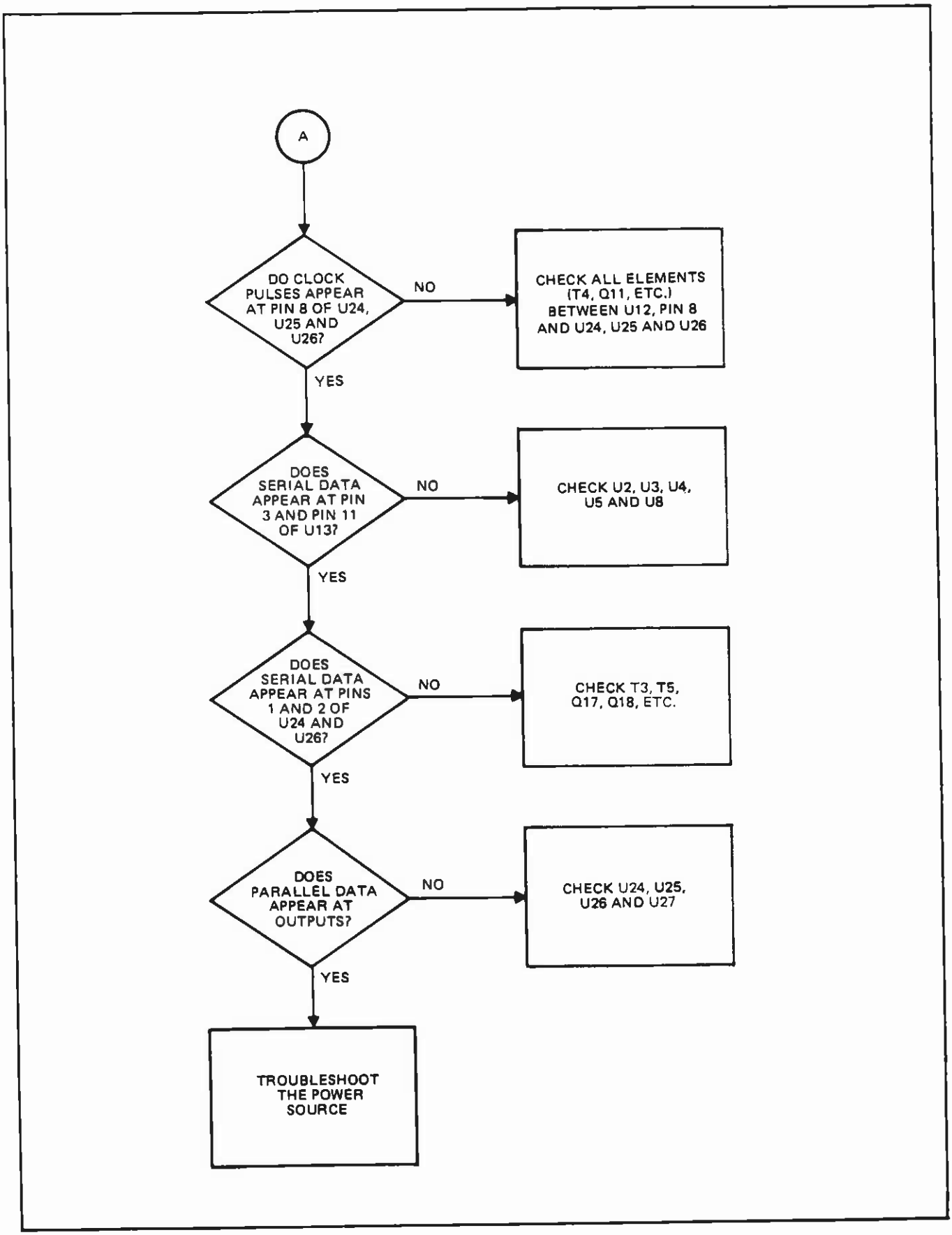


Table 6-6. TROUBLESHOOTING CHART, DATA ERRORS AT PARALLEL OUTPUTS

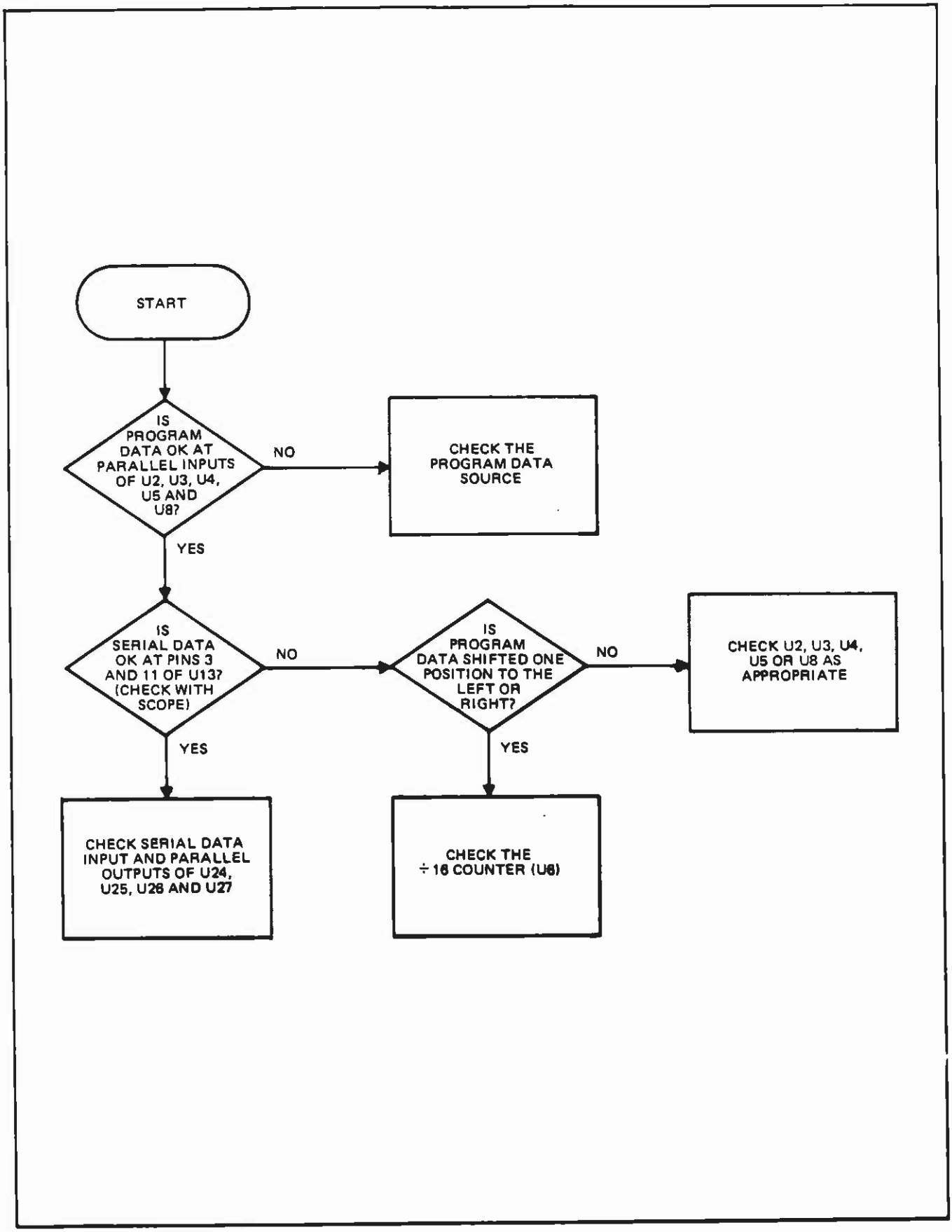


Table 6-7. TROUBLESHOOTING CHART, NO COMPLEMENTING OF BINARY DATA

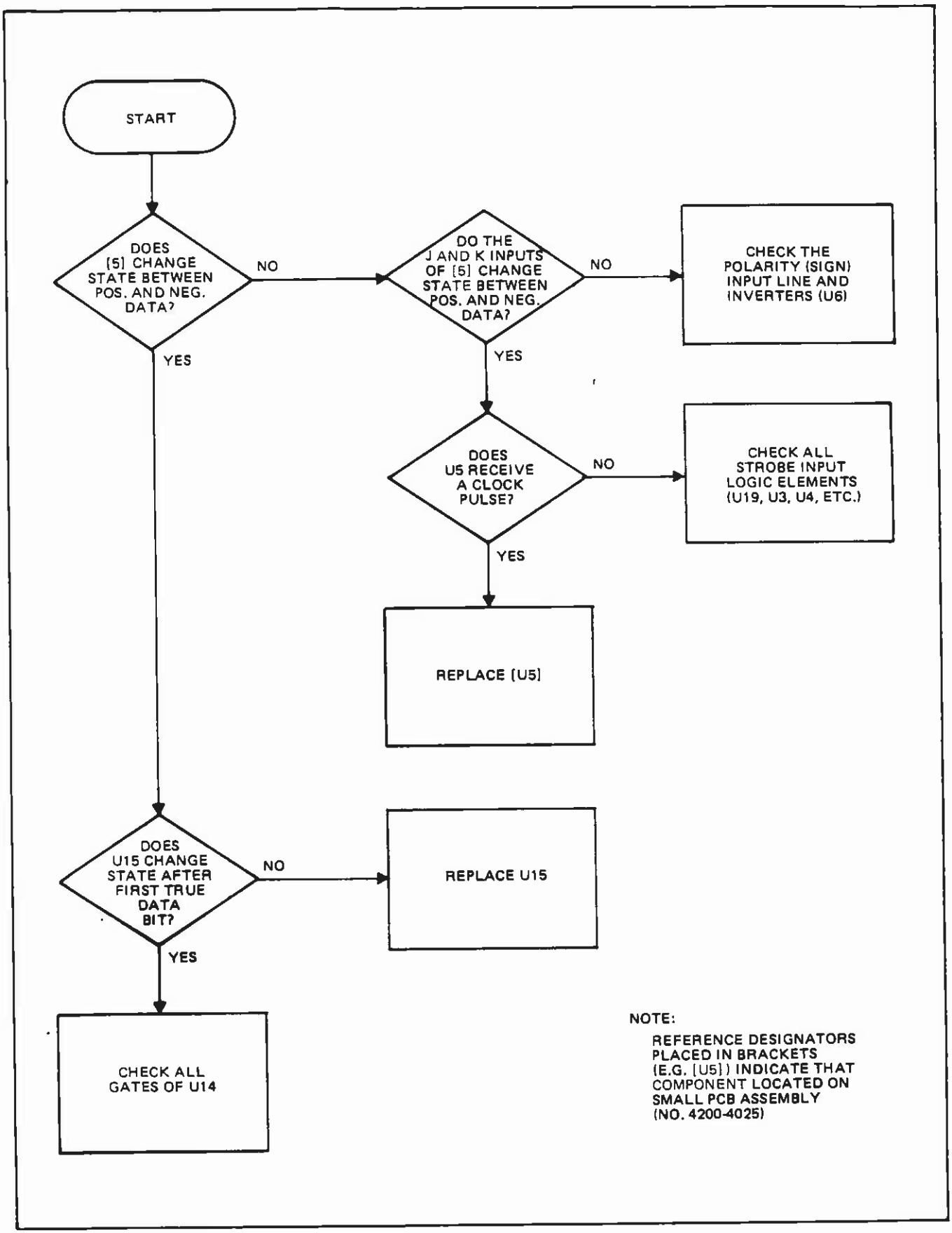


Table 6-8. TROUBLESHOOTING CHART, NO ASYNCHRONOUS STANDBY

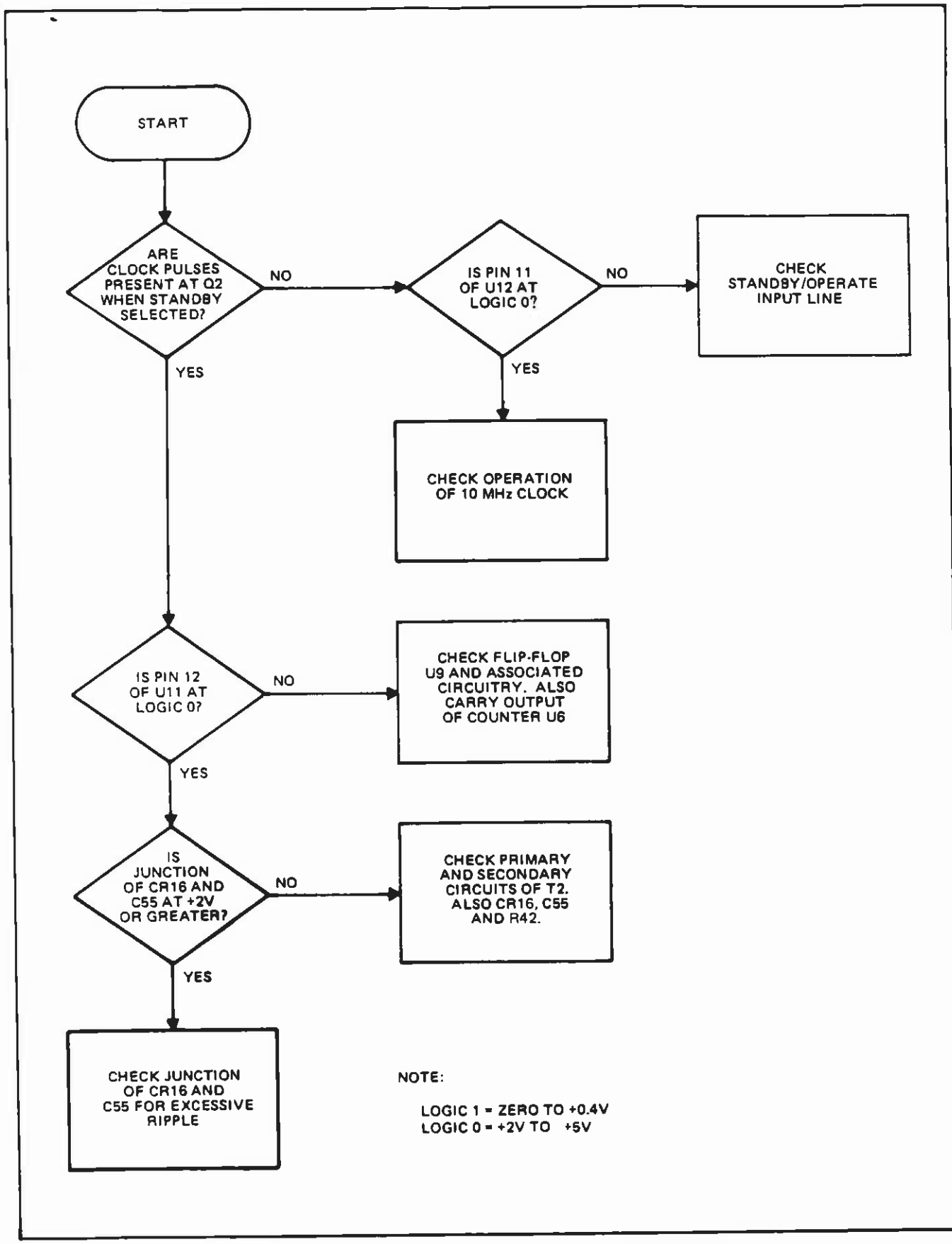


Table 6-9. TROUBLESHOOTING CHART, NO CURRENT LIMIT FLAG

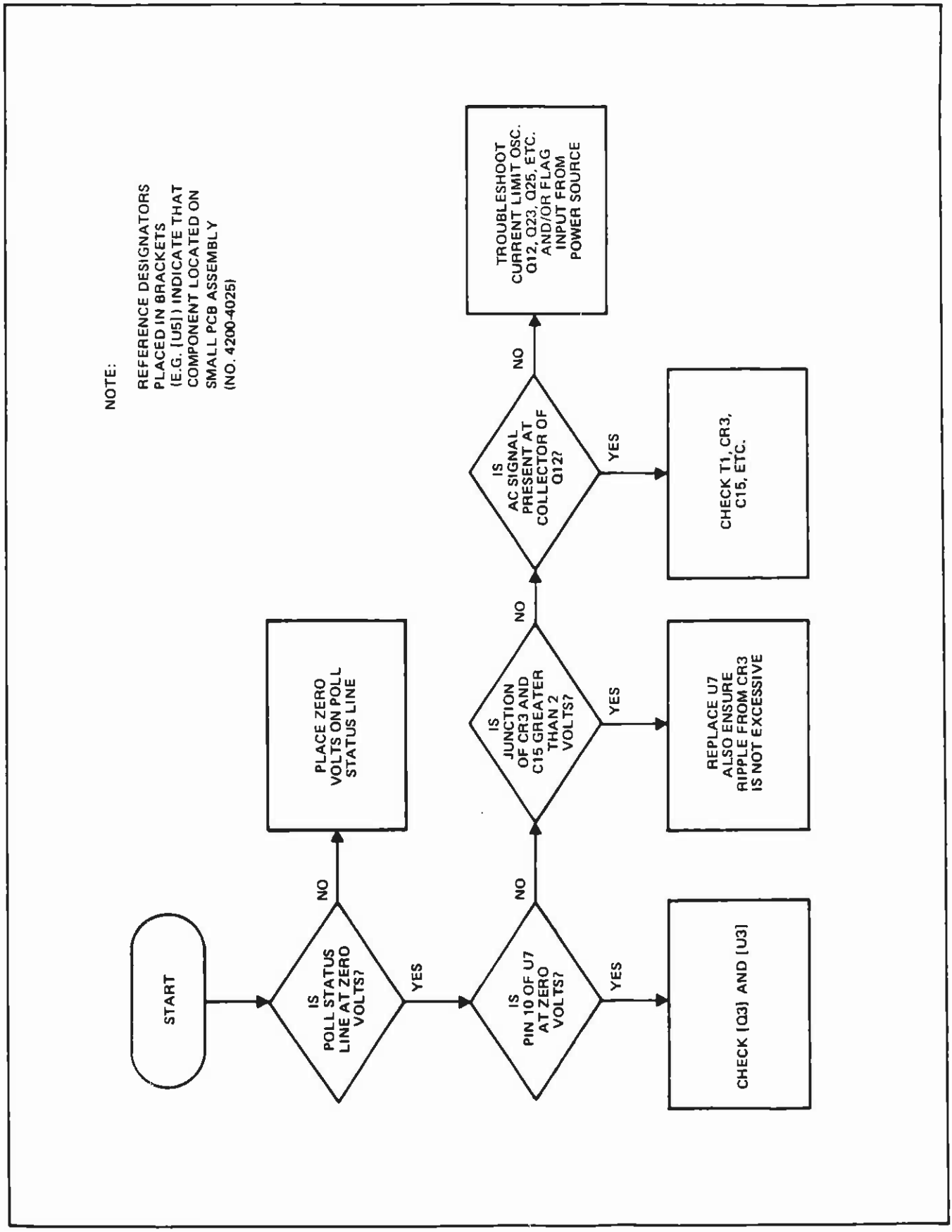


Table 6-10. TROUBLESHOOTING CHART, NO POWER FAIL AND/OR ABNORMAL STATUS FLAGS